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The IRE "Affiliate" Plan—A New Venture in Engineering Society Structure and Service

W. R. G. BAKER, *Chairman IRE Professional Groups Committee*

On January 4, 1957 the IRE Board of Directors arrived at a decision which may in time prove to be one of the most far-reaching in its 45-year history. On that date the Board adopted a plan which will enable non-IRE members whose main professional interests lie outside the sphere of IRE activities to become affiliated with certain of the IRE Professional Groups *without* first having to join the IRE itself.

This plan is aimed at those specialists in other fields of science and technology whose work touches upon our own electronics and communications field only in specialized areas. In effect, the IRE is extending the specialized services of its Professional Groups to every field of science and engineering.

An outstanding example of where these services are needed may be found in the case of the medical and biological sciences. At the present time some 1400 IRE members enjoy the privileges of membership in the Professional Group on Medical Electronics. And yet there are hundreds, perhaps thousands, of medical doctors, biologists, and others to whom the activities of this Group would be of interest and value. Both they and the Group would benefit from their participation. To require these persons, who have no interest in radio engineering, to join the IRE in order to join the Group is unreasonable, and probably futile as well. In fact, it was largely to provide an answer to this particular problem that the "Affiliate" Plan was first conceived, although it pertains to other fields as well, such as Computers, etc.

The "Affiliate" Plan is admittedly an experiment. So far as is known, no other society has ever tried a similar scheme. The Board of Directors feels strongly that the benefits afforded by the plan justify the risk that some persons who should join the IRE will instead become Affiliates. To minimize this risk, the plan has been carefully worked out along the following lines:

1) Participation in the Plan is at the option of each Professional Group. It is not expected that all Groups will adopt it; only those which feel it serves a need in their particular field.

2) Each Group interested in initiating the "Affiliate" Plan must submit to the Chairman of the Professional Groups Committee a list of accredited organizations which has been selected and approved by its Administrative Committee, for official approval by the IRE Executive Committee.

3) To be an Affiliate of a Professional Group, a person must belong to an accredited organization approved by that Group and the IRE Executive Committee. Moreover, he shall not have been an IRE member during the five years prior to his application. He may affiliate with more than one Group, provided the accredited organization to which he belongs is recognized by the Groups concerned.

4) The fee for Affiliates shall be the assessment fee of the Group, plus $4.50. The latter covers IRE subsidies to the Group, Professional Group overhead expenses borne by IRE Headquarters, and 50 cents which is to be rebated to IRE Sections for mailing and meeting costs.

5) An Affiliate will be entitled to receive the TRANSACTIONS of his Group and that part of the IRE NATIONAL CONVENTION RECORD pertaining to his Group. He will be eligible for a Group award, and may attend local or national meetings of the Group by payment of charges assessed Group members.

6) An Affiliate cannot serve in an elective office in the Group or Group Chapter, nor vote for candidates for these offices.

7) An Affiliate may hold an appointive office in the Group or Group Chapter.

8) An Affiliate may not receive any IRE benefits that are derived through IRE membership, except as authorized by the Executive Committee.

The "Affiliate" Plan is a bold and farsighted venture; one that recognizes and provides for the rapidly spreading influence of electronics in every walk of scientific and technological life, and one that enables the IRE to further its aims as a professional engineering society—the advancement of radio engineering and related fields of engineering and science.

A Time-Sequential Tabular Analysis of Flip-Flop Logical Operation*

GENE W. ARANT†

Summary—In examining flip-flop response the principal concern of the logical designer is to find what input signals must be applied to the flip-flop in order to produce the output conditions that are desired. Equation methods of analysis and a time-sequential tabular method of analysis are described, and some advantages of the tabular method are pointed out.

Introduction

A RATHER common problem is the logical design of a digital computer network, consisting of flip-flops and gates, which is to be operated in a sequential cycle including a number of separate successive time intervals.[1] The flip-flops drive the gates which in turn supply input signals to the flip-flops, and although other input and output signals are involved in the network their analysis presents no unique problem. The network must exhibit the correct logical response to information conditions which may exist during any time interval; hence, response requirements for the various time intervals may be lumped together for design purposes as constituting a single set of requirements. Either Boolean equations or tabular methods of analysis may be used.

One important phase of the problem may be described with reference to a single flip-flop. There is provided as the starting information a statement of the response which the particular flip-flop is required to exhibit to each of various possible information conditions. It then becomes the task of the logical designer to design gates which will supply correct input signals to the flip-flop.

Although the usual description[2,3] of flip-flop logical operation is a table or equation specifying the observed responses to various input conditions, it is apparent that what the logical designer needs is essentially an inverse representation of the flip-flop performance characteristic. That is, the logical designer needs a representation of the flip-flop indicating the input signals which must be supplied in order to produce a desired effect upon the stable state of the flip-flop.

* Manuscript received by the PGEC, October 26, 1955; revised manuscript received, December 22, 1956. The paper describes theoretical developments with which the author became familiar while employed as a patent attorney at Hughes Aircraft Co., Culver City, Calif., and The Ramo-Wooldridge Corp., Los Angeles, Calif.

† Patent lawyer, 19 Pine Ave., Long Beach, Calif.

[1] J. R. Harris, "A transistor shift register and serial adder," PROC. IRE, vol. 40, pp. 1597–1602; November, 1952.

[2] E. C. Nelson, "Algebraic theory for use in digital computer design," IRE TRANS., vol. EC-3, pp. 12–21; September, 1954.

[3] J. A. Postley, "A method for the evaluation of a system of Boolean algebraic equations," *Mathematical Tables and Other Aids to Computation*, vol. IX, 49, pp. 5–8; January, 1955.

Equation Analysis

The functional requirements placed upon a flip-flop in any time interval may be represented in a generalized form by the following:

$$Q_n = Q_{n-1}X_{n-1} + \overline{Q}_{n-1}Y_{n-1}. \tag{1}$$

Another way of saying it is that (1) indicates the information required to be represented by the stable state of the flip-flop. In (1) Q_{n-1} represents a binary digit, or bit, of information which is presently stored in the particular flip-flop and which has possible values of 1 and 0. $\overline{Q}_{n-1}$ represents the binary complement of Q_{n-1}. X_{n-1} and Y_{n-1} are functions of other information then available in the network, and Q_n is the new bit of information which must be formed by the gates and stored in the flip-flop in the ensuing time interval.

Of particular interest is the "triggering" flip-flop which has two separately triggerable input circuits, and which reliably responds to the simultaneous pulsing of both inputs to change from one to the other of its stable states. Solving (1) and the flip-flop response equation[4] simultaneously, several solutions for the input functions may be obtained as follows, where J and K respectively represent signals applied to the two input circuits:

$$\begin{aligned} J_{n-1} &= Q_n = Q_{n-1}X_{n-1} + \overline{Q}_{n-1}Y_{n-1} \\ K_{n-1} &= \overline{Q}_n = Q_{n-1}\overline{X}_{n-1} + \overline{Q}_{n-1}\overline{Y}_{n-1}. \end{aligned} \tag{2}$$

Eq. (2) implies the generation of the new bit of information entirely within the gates and its subsequent transfer from the gates to the flip-flop. In the physical realization of (2) the function for J may be generated by one gating circuit while the function for K is simultaneously generated by a second and separate gating circuit; or only a single function may be developed in a logical gate and then supplied to a complementer device for producing a pair of signals respectively representing the function and its complement. Note that insofar as the flip-flop itself is concerned, (2) also corresponds to information shifting as normally accomplished within a shifting register.

$$\begin{aligned} J_{n-1} &= \overline{Q}_{n-1}Y_{n-1} \\ K_{n-1} &= Q_{n-1}\overline{X}_{n-1}. \end{aligned} \tag{3}$$

Eq. (3) is a simplification of (2), however, the functions for J and K are no longer mutually complementary. The

[4] Nelson, *op. cit.*, Postley, *op. cit.*

physical realization of (3) therefore requires two separate gating circuits.

$$J_{n-1} = Y_{n-1}$$
$$K_{n-1} = \overline{X}_{n-1}. \tag{4}$$

Eq. (4) is a further simplification[5] in which use is made of the fact that the flip-flop responds with knowledge of its existing state. The physical realization of (4) also requires two separate gating circuits except in special cases where either one or both of the functions $\overline{X}$ and Y is a function of a single binary variable and hence directly available without the need for being synthesized in a special gate.

$$J_{n-1} = K_{n-1} = Q_{n-1}\overline{X}_{n-1} + \overline{Q}_{n-1}Y_{n-1}. \tag{5}$$

Eq. (5) represents the special case where the two input circuits are physically connected together and controlled by a single input function.

Also of interest is the "set-reset" flip-flop which is like the "triggering" flip-flop except that it does not reliably respond to the simultaneous pulsing of both its inputs and must, therefore, be subject to the restriction that only one of its inputs may be pulsed in any time interval. Input functions according to (5) cannot, therefore, be used, and input functions according to (4) can be used only if Y and $\overline{X}$ are never simultaneously 1 (as for example, in the carry flip-flop for a binary adder or subtracter). The set-reset flip-flop may be converted to a triggering flip-flop by an appropriate feedback gate connected from each of its outputs to the opposite input. Input functions may then be supplied in accordance with (3), which corresponds to the simplified input functions of (4) plus the feedback terms.

Tabular Analysis

If the functional requirements represented by (1) are stated in tabular form it becomes convenient to represent the flip-flop characteristic in tabular form also. Thus Table I specifies for the "triggering" flip-flop the

TABLE I

Necessary and Sufficient Input Signals for the Triggering Flip-Flop

Q_{n-1}	Q_n	J_{n-1}	K_{n-1}
0	0	0	
0	1	1	
1	0		1
1	1		0

input signals required to produce any desired effect upon its stable state. Symbol Q representing the stable state of the flip-flop has two possible values designated as binary 1 and 0, while J and K respectively represent signals applied to the two input circuits and are assigned binary values representing pulse or no pulse. The independent variable is the desired change (or no change) in stable state. Blank spaces in the J and K columns indicate that either a binary 1 or 0 may be used. Table I has three other equivalent forms obtainable by changing the binary designation of the stable state, the input signals, or both. It will be noted that Table I is not merely the inverse of the usual description of flip-flop response, but is somewhat more simplified.

The use of the time-sequential tabular method of analysis in which the tabular statement of functional requirements and the tabular description of flip-flop response are effectively combined[6] is illustrated by Table II, an example of a counter which continuously cycles through the 5 states—000—110—010—001—100.

TABLE II

Time Intervals						Triggering Flip-Flop Input Signals					
$n-1$			n								
QA	QB	QC	QA	QB	QC	JA	KA	JB	KB	JC	KC
0	0	0	1	1	0	1		1		0	
1	1	0	0	1	0		1		0	0	
0	1	0	0	0	1	0			1	1	
0	0	1	1	0	0	1		0			1
1	0	0	0	0	0		1	0		0	

The zeros and ones indicate the states of the three triggering flip-flops QA, QB, and QC in each count. The following equations are easily derived:

$$JA = \overline{B}$$
$$KA = \text{"1"} \text{ (or } A \text{ or } \overline{C})$$

$$JB = \overline{AC}$$
$$KB = \overline{A}$$

$$JC = \overline{A}B$$
$$KC = \text{"1"} \text{ (or } \overline{A} \text{ or } \overline{B} \text{ or } C)$$

where the time subscripts have been omitted since only simultaneous gating[7,8] is involved.

Comparison of Methods

In general, the choice of a method of analysis is influenced by whether or not all of the possible combinations of values of the information variables from which the input functions are to be formed may exist and need to be considered. In other words, the question is whether the computer must be designed to respond to

[5] First proposed at Hughes Aircraft Co. by Dr. Eldred C. Nelson in 1951.

[6] This method was first used at Hughes Aircraft Co. by John V. Blankenbaker in 1953. Mr. Blankenbaker has also supplied the particular illustration shown in Table II.

[7] W. V. Quine, "The problem of simplifying truth-functions," *Amer. Math. Monthly*, vol. 59, pp. 521–531; October, 1952.

[8] R. K. Richards, "Arithmetic Operations in Digital Computers," D. Van Nostrand Co., Inc., New York, N. Y., pp. 51–80; 1955.

all possible information conditions, or to less than all.

If all possible information conditions must be considered in the analysis, the simplest possible solutions for the flip-flop input functions may be obtained either by the described tabular method or by the described equation method. The tabular method has the advantage of simplicity and may for that reason be preferred.

If the analysis includes less than all of the possible information conditions the tabular method will again yield the simplest possible solutions. Described equation method may not do so, however, as is shown by deriving the input functions for flip-flop QB of the example. A general expression [like (1)] for the required state of flip-flop QB may be written from Table II:

$$QB_n = \overline{A}_{n-1}\overline{B}_{n-1}\overline{C}_{n-1} + A_{n-1}B_{n-1}\overline{C}_{n-1}$$
$$= \overline{B}_{n-1}\overline{A}_{n-1}\overline{C}_{n-1} + B_{n-1}A_{n-1}\overline{C}_{n-1}$$

and in accordance with (1):

$$X = A\overline{C}$$
$$Y = \overline{AC}$$

where the time subscripts have again been dropped. Hence, the simplified input functions according to (4) become:

$$JB = Y = \overline{AC}$$
$$KB = \overline{X} = \overline{A} + C.$$

It is apparent that the expression for KB derived by the tabular method is simpler as it includes only the term $\overline{A}$.

Where less than all of the possible information conditions need to be considered, the simplest possible solutions for the flip-flop input functions may nevertheless be obtained by means of a more elaborate equation analysis. The procedure involves writing one equation for all of the information conditions to which a response is required and an additional equation for each of the other information conditions, the equations then being solved simultaneously. On a comparative basis, however, the described tabular analysis appears to be a far more efficient working tool.

Acknowledgment

The author gratefully acknowledges the suggestions of Dr. Eldred C. Nelson, Lowell D. Amdahl, and Edward J. Schneberger of The Ramo-Wooldridge Corporation; and John V. Blankenbaker of Massachusetts Institute of Technology.

Dynamic Accuracy as a Design Criterion of Linear Electronic-Analog Differential Analyzers*

AMOS NATHAN†

Summary—**A frequency error analysis of computing elements is presented which leads to a definition of their dynamic accuracy. The concept of a computing transfer function is introduced for this purpose, permitting the evaluation of an effective bandwidth, the latter being connected with the variance of the output for wideband inputs. Limited bandwidth is considered as equivalent to finite resolution and thus to an additional effective error. Single frequency errors are dealt with separately and are shown to be of minor importance. Suitable optimalization of dynamic accuracy yields parameters of design and performance such as optimum computing time and required base amplifier gain.**

The theory is applied to integrators and adders with base amplifiers of direct and of capacitive coupling.

Introduction

THE BASIC specifications of differential analyzers consist of the required accuracy and range of computing times. The problem of the dynamic accuracy of a computing setup for the solution of linear differential equations has been solved by Macnee[1,2] who considers the perturbations of the roots of the differential equation which are caused by the physical characteristics of the computing elements. His theory is invaluable in the direct prediction of errors for given setups. For all but the simplest problems, however, it yields qualitative results only. Representative setups; *i.e.*, representative differential equations, determine criteria of design. It is somewhat difficult to say which problems are typical and an alternative approach may be desirable. The nonlinear case has also been discussed.[3,4]

The concept of dynamic accuracy as commonly used is rather vague. Here the performance of isolated computing elements operating upon representative inputs is considered and the error associated with the effective bandwidth, as recently introduced,[5] is used to define dy-

* Manuscript received by the PGEC, December 10, 1955; revised manuscript received, March 1, 1957.

† Israel Inst. Tech., Haifa, Israel.

[1] A. B. Macnee, "An electronic differential analyzer," PROC. IRE, vol. 37, pp. 1315–1324; November, 1949.

[2] A. B. Macnee, "Some limitations on the accuracy of electronic differential analyzers," PROC. IRE, vol. 40, pp. 303–308; March, 1952.

[3] F. J. Murray, "Mathematical Error Analysis for Continuous Computers," Project Cyclone Symposium II, Part 2, Reeves Instrument Corp., New York, N. Y., pp. 139–146; 1952.

[4] K. S. Miller and F. V. Murray, "A mathematical basis for an error analysis of differential analyzers," *J. Math. Phys.*, vol. 32, pp. 136–163; July–October, 1953.

[5] A. Nathan, "A note on bandwidth," PROC. IRE, vol. 44, pp. 788–790; June, 1956. (See also "Correction," PROC. IRE, vol. 45, p. 65; January, 1957.)

namic accuracy. It is shown in principle and explicitly in examples how to determine this quantity.

Once the applicability of the definition of dynamic accuracy has been accepted the importance of its determination is clear; parameters of design required to meet given specifications can be based on it and its optimalization yields information about the desirable value of fundamental quantities such as the amplification and the gain-bandwidth product of base amplifiers.

Representative Inputs

A computing element has to operate upon a variety of input signals. The errors introduced by its imperfections cannot be determined unless these signals be specified or the complete setup of the computing scheme be known. Some essential arbitrariness is seen to be involved at the very outset of any general theory of the accuracy of computing elements. At the basis of such a theory either some setups or else some inputs must be regarded as representative, and its success will largely depend upon the judicious choice of these. It must be borne in mind that cases may arise which deviate significantly from these assumptions; results of the theory must therefore not be taken too literally.

We intend to develop a theory based on consideration of typical inputs. Now such inputs may be represented in the time or in the frequency domain. The time dependent input represents directly the variable on which a mathematical operation is performed by the element. Indeed, time is the only independent variable in electronic analog computers; frequency representation is more convenient in the description of computing elements. Thus, a transfer function is physically more readily interpreted than equivalent impulse response.

In transforming the input from time to frequency dependence, note that knowledge of the march of the complete time function is required, from $t=-\infty$ to $t=+\infty$. The computing time per solution of a differential analyzer is limited to $t=0 \cdots T$, and only those values of the input that lie between $t=-\epsilon$ and $t=T$, where ϵ is a small positive quantity, should affect the output during $0 \cdots T$. Although later we shall adopt a slightly different approach, it will now be convenient to assume zero input for $t<0$ and for $t>T$.

Let us, therefore, examine several truncated functions which are to be considered as examples of inputs to computing elements. Table I (next page) contains several such functions and their power spectra. Here we have set $T=1$. The spectra are seen to fall roughly into one of two groups: 1) wide-band spectra which resemble in character that of the sampling function, no. 4) of the table, [1), 2), 3), and 4)], and 2) those that have one pronounced peak [5) and 6)]; the latter resemble the spectrum of a continuous sine wave). It will be shown that the requirements imposed by the first group of signals are usually much more severe than those of the second. Criteria of design and performance will, therefore, be based primarily on inputs of the first group.

Wide-Band Inputs

The performance of linear computing elements with wide-band inputs can be described by their effective bandwidth, a concept which was introduced in a recent paper,[5] and which serves to compare the operation of a given network N with that of an "ideal" network I, with this type of input. The general idea is as follows.

Take the band-limited input signal[6]

$$\bar{e}_i = \bar{e}_1 \triangleq \begin{cases} \epsilon^{j\omega_0 t}, & |\omega| \leqq \omega_m \\ 0, & |\omega| > \omega_m \end{cases} \tag{1a}$$

which corresponds to

$$e_i(t-t_0) = e_1(t-t_0) = \frac{\omega_m}{\pi} \frac{\sin \omega_m(t-t_0)}{\omega_m(t-t_0)}$$

$$\triangleq \frac{\omega_m}{\pi} \operatorname{sinc} \omega_m(t-t_0); \tag{1b}$$

and use it as input to both N and I. (In the reference only $t_0=0$ was considered.) In comparing the outputs we permit the adjustment of the gain of an element, in order to obtain the best agreement; two elements would, for example, be considered as equivalent if the ratio of their transfer functions is a real constant not necessarily equal to one. Thus, we consider the transfer function of I as given, except for a multiplicative real constant α. The variance of the outputs provides a a measure of their agreement and its minimum with respect to α is defined as the effective—or rms error squared, ϵ_1^2. It turns out to be

$$\epsilon_1^2(\omega_m) = \frac{\int |\overline{H}_I|^2 d\omega \int |\overline{H}_N|^2 d\omega - \left[\int \operatorname{Re}(\overline{H}_I \overline{H}_N^*) d\omega\right]^2}{\int |\overline{H}_I|^2 d\omega \int |\overline{H}_N|^2 d\omega} \tag{2a}$$

where the integrations extend from 0 to ω_m. $\overline{H}_I$, $\overline{H}_N$ are the transfer functions of I and N, respectively, and ω_m is defined as the *effective* (angular) *bandwidth* of N with respect to I associated with error ϵ_1.

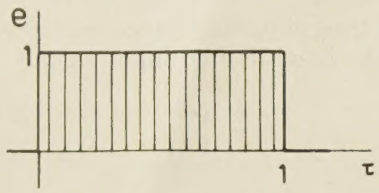
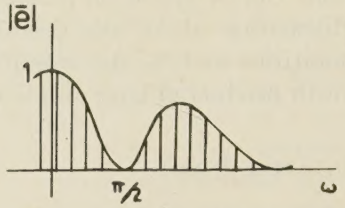
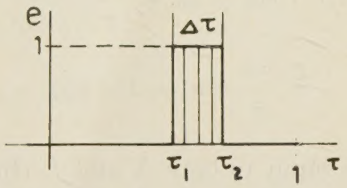
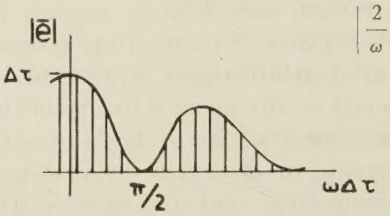
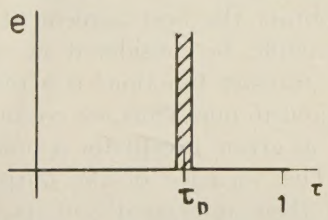
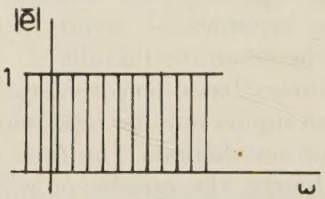
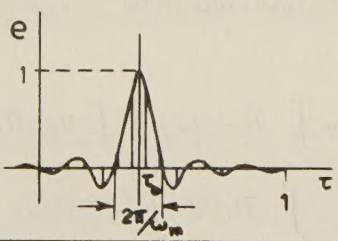
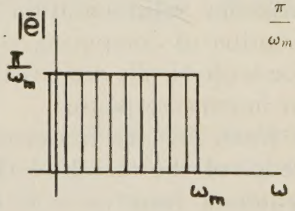
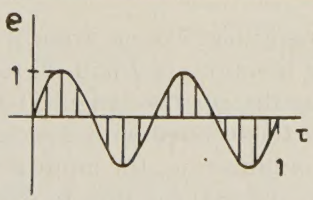
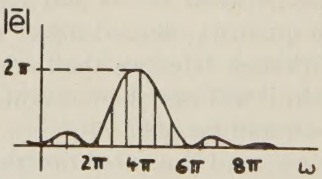
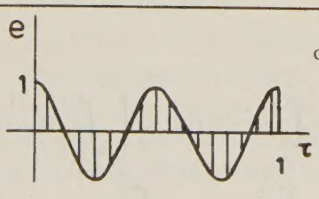
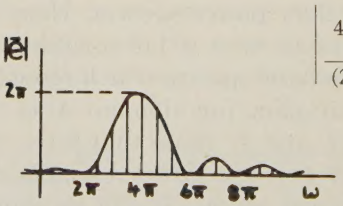
In the limit of infinite ω_m the input is proportional to a delta function and (2a) can then be expressed in terms of the impulse responses $W_I(t)$ and $W_N(t)$ of I and N, yielding

$$\epsilon_{1\infty}^2 = \frac{\int_0^\infty W_I^2(t)dt \int_0^\infty W_N^2(t)dt - \left[\int_0^\infty W_I(t) W_N(t) dt\right]^2}{\int_0^\infty W_I^2(t)dt \int_0^\infty W_N^2(t)dt}. \tag{2b}$$

[6] These symbols will be used throughout this paper:
= identically equal
$\triangleq$ equal by definition
$\cong$ approximately equal
$\sim$ very roughly equal
$\propto$ proportional
$\delta(t)$ unit impulse
$\mathbf{1}(t)$ unit step.

TABLE I

SPECTRA OF TRUNCATED FUNCTIONS

№	$e(\tau)$	$\lvert\bar{e}\rvert$
1)	 $1(\tau)1(1-\tau)$	 $\left\lvert\frac{2}{\omega}\sin\frac{\omega}{2}\right\rvert$
2)	 $1(\tau-\tau_1)1(\tau_2-\tau)$ $\Delta\tau \triangleq \tau_2-\tau_1<1$	 $\left\lvert\frac{2}{\omega}\sin\frac{\omega\Delta l}{2}\right\rvert$
3)	 $\delta(\tau-\tau_0)$	 1
4)	 $\frac{\sin\omega_m(\tau-\tau_0)}{\omega_m(\tau-\tau_0)}$ (not truncated)	 $\frac{\pi}{\omega_m}1(\omega+\omega_m)1(\omega_m-\omega)$
5)	 $\sin 2\pi N\tau 1(\tau)1(1-\tau)$ ($N=2$ sketched)	 $\left\lvert\frac{2\omega\sin\frac{\omega}{2}}{(2\pi N)^2-\omega^2}\right\rvert$
6)	 $\cos 2\pi N\tau 1(\tau)1(1-\tau)$ ($N=2$ sketched)	 $\left\lvert\frac{4\pi N\sin\frac{\omega}{2}}{(2\pi N)^2-\omega^2}\right\rvert$

SINGLE-FREQUENCY INPUTS

The other extreme consists of a steady-state sine input, $\epsilon^{j\omega_0 t}$, corresponding to an impulse $\delta(\omega-\omega_0)$ in the frequency domain. The complex outputs of I and N are now $\overline{H}_I(j\omega_0)$ and $\overline{H}_N(j\omega_0)$. Writing $\alpha\overline{H}_I$ for $\overline{H}_I$ as before, the output error is $\overline{E}=\alpha\overline{H}_I-\overline{H}_N$ (Fig. 1). This

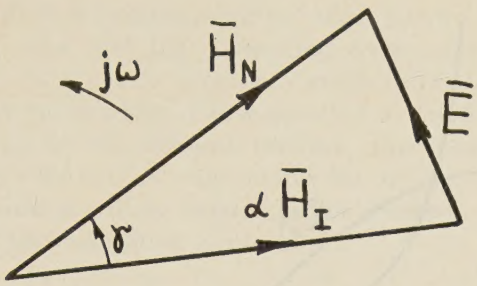


Fig. 1.

expression attains its minimum value for $\alpha|\overline{H}_I| \cong |\overline{H}_N|$ provided the fractional minimum error is small, which is then given by

$$e = \frac{|\overline{E}|_{\min}}{|\overline{H}_N|} \cong \gamma \triangleq \measuredangle(\overline{H}_I, \overline{H}_N); \tag{3}$$

i.e., the fractional single-frequency error is approximately equal to the phase error of N with respect to I. As such it is usually specified for amplifiers and for adders only; we now recognize its general importance.

Note α is a function of frequency. What now, if two frequencies, say ω_1 and ω_2, must be handled simultaneously by the computing elements, or if we do not allow a readjustment of gain for error compensation when changing the input frequency from ω_1 to ω_2? If we adjust α for minimum error at $\omega_0 = \omega_1$, which requires

$$\alpha(\omega_1)\,|\overline{H}_I(\omega_1)| = |\overline{H}_N(\omega_1)|$$

(3) will apply at this frequency. At ω_2, however, the error will no longer be given solely by the phase difference, since, in general, $\alpha(\omega_1)|\overline{H}_I(\omega_2)| \neq |\overline{H}_N(\omega_2)|$. Thus, the error for ω_2 will be larger than that given by (3). These remarks show the limited usefulness of the present results and the advantage of the simultaneous consideration of a whole band of frequencies as in the preceding section, where equal weight was given to all frequencies in the band 0 to ω_m.

It will be convenient to normalize the time scale at this point before proceeding to apply these concepts to differential analyzers.

Change of Scale

Let us change the time scale from real time t to a normalized time τ defined by

$$\tau \triangleq t/T.$$

The computing interval in τ is thus always $0 \cdots 1$. We have, for example, $e_i(\tau) = e_{i_t}(T\tau)$, where the suffix t denotes quantities on the old scale.

Letting w denote the angular frequency in τ, $w = \omega T$. The scale of the impulse response may be changed as well, writing

$$W(\tau) \triangleq TW_t(T_\tau)$$

in order to ensure that for the outputs

$$e_0(\tau) = e_{0t}(T\tau).$$

These relations affect the transfer function as follows,

$$\overline{H}(p) = \overline{H}_t(P/T).$$

The last two relations are proved in Appendix I.

From now on we shall mostly work with normalized time.

The Computing Transfer Function

The bandwidth relation (2) is not directly applicable to differential analyzers where we are interested in the errors which occur during the computing time only; only that part of signals which lies within $\tau = 0 \cdots 1$ must be considered. The assumed *input* can be made to meet this requirement well enough; writing $\omega_m t = \tau$ it is centered on τ_0 and goes to zero fairly rapidly both before and after; it will, therefore, fall almost wholly within or near the allowed interval, provided $0 \leqq \tau_0 \leqq 1$. This need not be so for the *output*. An ideal integrator, for example, will hold the integral of a delta function input for all eternity, yet it is only the truncated; *i.e.*, $\tau = 0 \cdots 1$, part of the output of element N that must be compared with that of I in forming the variance. Transfer function $\overline{H}$, however, may provide nonzero output at $\tau > 1$, through $\overline{H}\bar{e}_i = \bar{e}_0$.

Let us replace $\overline{H}(p)$ by the computing transfer function $\overline{C}(p)$ which will now be defined. First, note that an element can be described either by its transfer function $\overline{H}$ or by its memory function, or impulse response, $W(\tau)$. In fact $\overline{W} = \overline{H}$. We now define the *computing memory* $c(\tau)$ as the truncated function

$$c(\tau) \triangleq W(\tau)1(1-\tau), \tag{4}$$

and the *computing transfer function* $\bar{c}(p)$ as its Fourier or Laplace transform. $W(\tau) = 0$ for $\tau < 0$; $c(\tau) = 0$ for $\tau < 0$ *and* for $\tau > 1$. The computing memory extends over unit duration. Provided the input is confined within $\tau = 0 \cdots 1$, $\overline{C}$ will generate the same output as $\overline{H}$ during this interval and may generate some additional output during $\tau = 1 \cdots 2$; the rest is silence. Formally, using the convolution integral, with $f_1(\tau) = e_i(\tau)\Lambda(\tau)\Lambda(1-\tau)$ as input and (4) as memory, the output becomes

$$\begin{aligned} e_0(\tau) &= \int_0^\tau f_1(t)c(\tau - t)dt \\ &= \int_0^\tau e_i(t)1(t)1(1-t)W(\tau - t)1(1-\tau+t)dt \\ &= \begin{cases} 0, & \tau \leqq 0; \\ \displaystyle\int_0^\tau e_i(t)W(\tau - t)dt, & 0 \leqq \tau \leqq 1; \\ \displaystyle\int_{\tau-1}^1 e_i(t)W(\tau - t)dt, & 1 \leqq \tau \leqq 2; \\ 0, & \tau \geqq 2. \end{cases} \end{aligned}$$

Returning now to the bandwidth relations (2), writing $e_i(\tau - \tau_0)$ for $e_i(t - t_0)$, τ for $\omega_m t$, τ_0 for $\omega_m t_0$, and w for ω in (1) and (2), and noting that practically all of input (1) occurs at or near $\tau = \tau_0$, we may replace the condi-

tion of confinement of e_i within $\tau = 0 \cdots 1$ by $0 \leqq \tau_0 \leqq 1$. We shall now use (2a) and (2b) for the calculation of errors in time limited computations by substituting $\overline{C}$ for $\overline{H}$ and c for W. It is easy to see that this procedure is accurate, if $\tau_0 = 0$ in test signal (1). Actually there is little justification for this additional requirement since the test signal could be centered on any instant within the computing interval with equal likelihood, but it is not considered worthwhile to rectify this deficiency, although this could be done by averaging over-all τ_0 from 0 to 1. In this connection note that requirement $\tau_0 = 0$ is superfluous in the consideration of computing elements of short-range memory such as adders or differentiators.

The relation between computing transfer function $\overline{C}$ and ordinary transfer function $\overline{H}$ is (Appendix II)

$$\overline{C}(p) = \overline{H}(p) - \epsilon^{-p}[\overline{W(\tau + 1)1(\tau)}]. \tag{5}$$

As examples, consider ideal adders and integrators. For an adder $W_t(t) = \delta(t)$, thus

$$W(\tau) = T\delta(T\tau) = \delta(\tau); \qquad c(\tau) = \delta(\tau);$$

and

$$\overline{C} = 1. \tag{6}$$

For an integrator

$$W_t(t) = 1(t); \qquad \overline{H}_t = \frac{1}{p};$$

and

$$W(\tau) = T1(T\tau) = T1(\tau); \qquad \overline{H} = T/p.$$

Thus

$$c(\tau) = T1(\tau)1(1 - \tau)$$

and

$$\overline{C} = \frac{T}{p}(1 - \epsilon^{-p}); \quad |\overline{C}| = 2\frac{T}{w}\left|\sin\frac{w}{2}\right|. \tag{7}$$

Note that $|\overline{C}(0)| = T$, whereas $|\overline{H}(0)|$ is infinite. Fig. 2 shows the absolute value of $\overline{H}$ and $\overline{C}$ for ideal integrators.

We are now in a position to calculate the effective bandwidth B_m as a function of the error ϵ_1. The presentation of this relationship is of importance in order to determine the best computing time of a setup. It is sometimes possible to estimate the salient frequencies expected in the solution of a problem; alternatively, once an approximate solution of a problem has been obtained, the spectra of the outputs which appear at all the computing elements can be estimated. This information allows an adjustment, or readjustment, of computing speed so that these spectra will fall into regions of small error; roughly speaking, computing speed should be such that signal frequencies fall within the pass band of the computing elements. It is suggested that curves of bandwidth vs error be supplied for all elements.

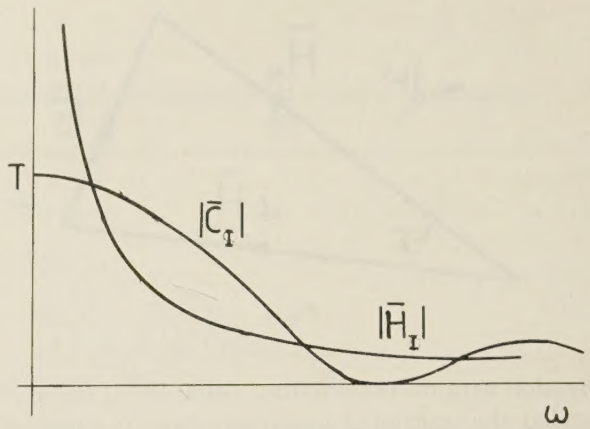


Fig. 2—Ordinary and computing transfer functions of an ideal integrator.

Dynamic Accuracy (DA)

Returning to our band-limited input test signal, ϵ_1 would provide a direct measure of DA; yet actual spectra may extend to infinity and we must now turn to a consideration of the effects of high-spectrum frequencies. Alternatively, we pose the question whether there is a criterion prescribing the required bandwidth.

The situation may be regarded as the cascade connection of two elements: M, a filter of bandwidth B_m, and N, the actual computing element. M introduces errors by suppressing frequencies; N, through inaccurate operation within B_m. The fractional rms error introduced by M will be denoted by ϵ_2; it depends on the nature of the input and on B_m. ϵ_1, as given by (2a), denotes the error of N. We define the *total error* as

$$\epsilon_{tot} \overset{\Delta}{=} \sqrt{\epsilon_1^2 + \epsilon_2^2}. \tag{8}$$

Although ϵ_2 could be determined by a consideration of an appropriate input test signal, such as a step function, a different approach will be preferred. If M were a filter with sharp cutoff, its (numerical) bandwidth B_m would allow it to pass without error $2B_m$ sampling pulses per unit time; *i.e.*, per computation. In this sense we may speak of a resolution $1/2B_m$ of M. We assume that ϵ_2 is proportional to this resolution and write

$$\epsilon_2 = \beta/2B_m. \tag{9}$$

With a resolution of $1/2B_m$ one can associate a maximum error squared of $(\pm 1/4B_m)^2$ which corresponds to an average of $\frac{1}{3}(1/4B_m)^2$. Equating this to ϵ_2^2 one obtains from (9) $\beta = 0.29$. Let us use $\beta = 0.20$ instead, thus allowing for the fact that M is a filter which cuts off gradually rather than sharply. Therefore

$$\epsilon_2^2 = 10^{-2}/B_m^2 = 0.40/w_m^2. \tag{9a}$$

These arguments for fixing β seem rather vague; fortunately it turns out that the results obtained in ordinary applications are quite insensitive to its exact value.

Errors of input components up to w_m are now included in ϵ_1, errors of higher components in ϵ_2; ϵ_1 eventually increases while ϵ_2 decreases with increasing w_m,

yet a shift in w_m corresponds to nothing but a changed point of view and the computing error must not be affected. As ϵ_{tot} is to provide a measure of this error, only that value where it is insensitive to small changes in w_m can be of physical interest; this happens at $d\epsilon_{tot}/dw_m = 0$; *i.e.*, at the minimum of ϵ_{tot}. Finally, this minimum will be *defined* as the *dynamic accuracy* (DA) of the computing element,

$$DA \triangleq \epsilon_{tot\,min}. \tag{10}$$

These considerations also settle the question as to when to use (2b) instead of (2a) in the calculation of DA. This will be permissible whenever $\epsilon_2^2 \ll \epsilon_1^2$ at the frequency which minimizes ϵ_{tot}. An example is furnished by an integrator having the error curves sketched in Fig. 3; here the minimum of ϵ_{tot} corresponds to $w = \infty$, where $\epsilon_2 = 0$, and DA follows from (2b), (8), (9), and (10). The case of an adder is sketched in Fig. 4; calculation of DA now requires the use of (2a).

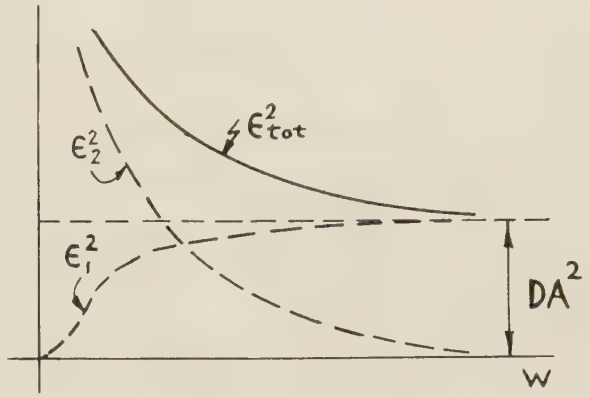


Fig. 3—Integrator error functions and dynamic accuracy.

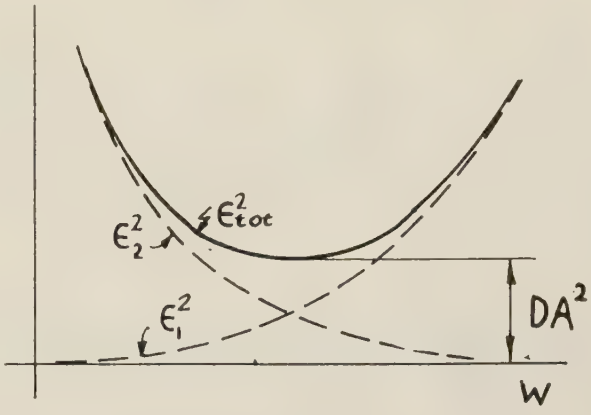


Fig. 4—Adder error functions and dynamic accuracy.

Applications

The Integrator

Consider an integrator consisting of a dc amplifier of gain $-A_i$ and time constant T_a, input resistance R and feedback capacitance C (Fig. 7). Taking into account two time-constants, $T_1 = T_a/A_i$ and $T_2 = A_i RC$, we have (Appendix III)

$$\overline{H}_N \propto \frac{1}{(p+a)(p+b)} \equiv \frac{1}{b-a}\left[\frac{1}{p+a} - \frac{1}{p+b}\right], \tag{11}$$

where

$$a \triangleq T/T_1; \qquad b \triangleq T/T_2; \qquad a \gg b. \tag{11a}$$

Note that T_1 is related to the gain-bandwidth product $(GB)_i$ of the base amplifier through

$$(GB)_i = A_i/2\pi T_a = 1/2\pi T_1. \tag{11b}$$

Because constant factors in the transfer functions are of no consequence in the sequel they will be freely omitted. The inverse transform is the impulse response $W_N(\tau)$; we use the truncated, $\tau = 0 \cdots 1$, part of it only and obtain (Fig. 5),

$$c_N(\tau) = (\epsilon^{-b\tau} - \epsilon^{-a\tau})1(\tau)1(1-\tau). \tag{12}$$

Next we calculate DA_i. The situation of Fig. 3 holds here; *i.e.*, $DA_i = \epsilon_1^{\infty}$. For small errors, $T_1 \ll T \ll T_2$; assuming also $T \gg T_a/k_i$, one obtains from (2b), (Appendix IV)

$$DA_i^2 \cong \frac{6+ab^2}{12a} = \frac{6\left(\frac{T_1}{T}\right) + \left(\frac{k_i}{A_i}\right)^2}{12}. \tag{13}$$

k_i is the integrator gain as defined by

$$k_i \triangleq T/RC. \tag{14}$$

Two cases must now be distinguished.

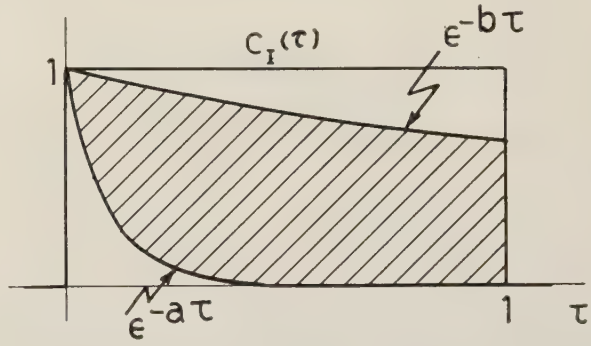


Fig. 5 -Integrator memory functions; C_I ideal, C_N imperfect (represented by ordinates through shaded area).

The Integrator with Fixed Input and Feedback Elements

Proper external gain is here obtained by adjustment of an input potentiometer, Fig. 6. To obtain the optimum computing time $T = T_0$, we solve $\partial DA_i^2/\partial T = 0$; *i.e.*, $T_0^3 = 3T_1T_2^2$ or $ab^2 = 3$. The solution is

$$T_0 \cong 1.44\sqrt[3]{T_1T_2^2} = 3T_1\left(\frac{A_i}{k_{i0}}\right)^2. \tag{15}$$

k_{i0} is defined by (14) with $T = T_0$ and does not include the gain of the potentiometer. With this value of T we obtain an optimum DA_i

$$DA_{i0} \cong 0.5\,\frac{k_{i0}}{A_i} \cong 0.72\sqrt[3]{\frac{T_1}{T_2}} = \frac{0.39}{\sqrt{(GB)_iT_2}}. \tag{16}$$

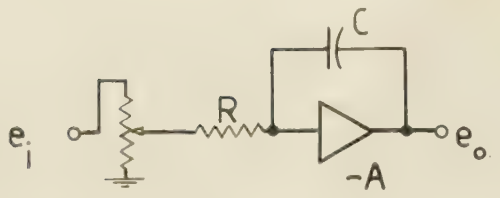


Fig. 6—Integrator with fixed input and feedback elements and adjustable gain.

From (13) and (16) follows

$$\left(\frac{DA_i}{DA_{i0}}\right)^2 \cong \frac{2+\left(\frac{T}{T_0}\right)^3}{3\left(\frac{T}{T_0}\right)}. \tag{16a}$$

This expression falls off fairly slowly to its minimum at T_0, but rises rather steeply for $T>T_0$. For example, at $T=T_0/20$, $DA_i\sim 3DA_{i0}$, whereas at $T=20T_0$, $DA_i\sim 10DA_{i0}$. Computing times much larger than T_0 should therefore be avoided, but considerably smaller times may be used without serious detriment.

The Integrator of Fixed Gain

We now demand constant external gain and achieve this condition by appropriate changes in the RC-product, Fig. 7. Thus

$$b = \frac{T}{T_2} = \frac{T}{A_i RC} = \frac{k_i}{A_i} = \text{const.}$$

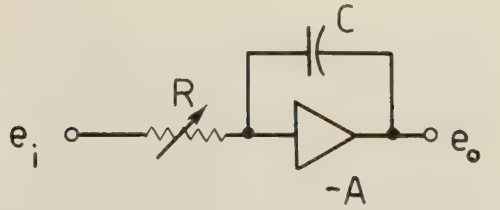


Fig. 7—Integrator with fixed gain and adjustable input resistance.

It follows from (13) that DA_i decreases with increasing T/T_1; it does so, however, more and more slowly. It is hardly worthwhile to increase T beyond

$$T_m = 6T_1\left(\frac{A_i}{k_i}\right)^2 = \frac{0.95}{(GB)_i}\left(\frac{A_i}{k_i}\right)^2 \cong \sqrt[3]{\frac{T_2^2}{(GB)_i}}, \tag{17}$$

which corresponds to a DA_i of 140 per cent of its limit for infinite T. The associated DA_i is

$$DA_{im} \cong 0.40\frac{k_i}{A_i} = 0.74\sqrt[3]{\frac{T_1}{T_2}} = \frac{0.39}{\sqrt[3]{(GB_i)T_2}}. \tag{18}$$

Moreover

$$\left(\frac{DA_i}{DA_{im}}\right)^2 = \frac{T+T_m}{2T}. \tag{18a}$$

The value of RC which is required for operation with $T=T_m$ is

$$(RC)_m = \frac{T_m}{k_i} = \frac{6A_i^2T_1}{k_i^3}. \tag{19}$$

In practice, the available RC-product is limited to some value $(RC)_{max}$. The relations derived in this section hold, therefore, for $k_i \geqq k'$ only, where

$$k' = \frac{T_m'}{(RC)_{max}} = \sqrt[3]{\frac{6A_i^2T_1}{(RC)_{max}}}. \tag{20}$$

T_m' denotes the value of T_m which corresponds to k'.

Smaller values of external gain can only be realized by operation according to the scheme of the previous section. It will then be advantageous to choose $k_i=k'$ and to obtain the balance of gain reduction by adjustment of the potentiometer. In order to obtain the appropriate dynamic accuracy DA_i'', we revert to (13) and obtain at $T=k_i(RC)_{max}$

$$DA_i'' \cong \sqrt[3]{\frac{6T_1+\left(\frac{k_i}{A_i}\right)^2 k_i(RC)_{max}}{12k_i(RC)_{max}}}$$

$$\cong \sqrt{\frac{T_1}{2k_i(RC)_{max}}} = 0.72\sqrt{\frac{T_1}{T}} \tag{21}$$

provided $k_i<\sim\frac{1}{2}k'$.

For fixed GB, the gain of the operational amplifier of an integrator should be made large, *provided* one operates with optimum computing time. If operation over a wide range of computing times T is required, the gain should be sufficient for good performance at the longest times; for shorter times, one may have to work with $T<T_m$ and, from (13), DA becomes a function of T and GB only; the gain can then be reduced without impairment of performance until T is about equal to the new value of T_m.

We shall regard the integrator with fixed gain as typical throughout the rest of this paper.

To review:

1) An integrator has an optimum computing time; this optimum is not critical.
2) Amplifier gain determines the value of optimum DA; the amplifier gain bandwidth product determines the available *range* of computing times.

A Numerical Example

Given:

$A = 2\times 10^4$; $T_a = 5\times 10^{-2}$ sec; $(RC)_{max} = 1$ sec.

It follows that

$$k' = \sqrt[3]{6\times 2\times 10^4\times 5\times 10^{-2}} = 18.$$

1) For $k_i=>k'$, $DA_m = 20/2.5\times 2\times 10^4 = 0.04$ per cent at $T=T_m=6\times 5\times 10^{-2}\times 2\times 10^4/20^2=15$ sec, and $RC=15/20=0.75$ sec <1 sec.

2) For $k_i = 5 < k'$,

$$DA_i = DA_i'' = \sqrt{5 \times 10^{-2} / 2 \times 5 \times 2 \times 10^4}$$

$= 0.05$ per cent at $T = 5$ sec.

The Isolated Adder

It turns out that an adder cannot function with a finite error unless the bandwidth of the input signal is limited. In this section we shall consider the performance of an isolated adder and in the next that of an adder in cascade with an integrator.

We approximate the transfer function of the adder by (Appendix III)

$$\overline{H}_N = \frac{1}{p + \dfrac{T}{T_3}}; \qquad T_3 \cong (1 + k_a)\frac{T_a}{A_a} = \frac{1 + k_a}{2\pi (GB)_a}.$$

T_a is again the time constant of the base amplifier, $-A_a$ its gain, and $-k_a = -R_f/R_i$ denotes the external gain of the adder. Thus

$$\overline{C}_N \cong \frac{1}{p + \dfrac{T}{T_3}} = \frac{1}{p + c} \quad \text{where} \quad c \triangleq \frac{T}{T_3}. \tag{22}$$

Moreover $\overline{C}_I = 1$.

If the input band be limited to $0 \cdots w_m$, we obtain for ϵ_1^2 (2a)

$$\epsilon_1^2 = \frac{\displaystyle\int_0^{w_m} |\overline{C}_N|^2 dw - \left[\mathrm{Re}\int_0^{w_m} \overline{C}_N^* dw\right]^2}{\displaystyle\int_0^{w_m} |\overline{C}_N|^2 dw}.$$

The integrations are straightforward and result in

$$1 - \frac{\arctan^2\left(\dfrac{w_m}{c}\right)}{\dfrac{w_m}{c}\arctan\left(\dfrac{w_m}{c}\right)}$$

and, provided

$$w_m/c \ll 1; \qquad i.e.,\ w_m \ll \frac{T}{T_3} = \frac{A_a}{1 + k_a}\cdot\frac{T}{T_a}$$

$$\epsilon_1^2 \cong \frac{1}{3}\, w_m^2 \left(\frac{T_3}{T}\right)^2. \tag{23}$$

Equivalently, we may say that the computing bandwidth $B_m = w_m/2\pi$ is given by

$$B_m \cong 0.28\,\frac{T}{T_3}\,\epsilon_1 = \frac{1.76}{1 + k_a}\,(GB)_a T \epsilon_1. \tag{23a}$$

The computing bandwidth is thus proportional to the GB product of the amplifier and to the computing time. Note that the frequencies and the bandwidth B_m are referred to the numerical time-scale τ.

We shall now determine the dynamic accuracy of the adder. For the total error (8) we have, using (9a) for ϵ_2,

$$\epsilon_{\mathrm{tot}}^2 = \epsilon_1^2 + \epsilon_2^2 = 0.58\left(\frac{T_3}{T}\right)^2 w_m^2 + \frac{0.40}{w_m^2}.$$

Now the minimum of $f(x) = ax + b/x$ is $2\sqrt{ab}$ at $x = \sqrt{a/b}$. The dynamic accuracy is, therefore,

$$DA_a = \epsilon_{\mathrm{tot\,min}} = \sqrt{2 \cdot 0.58\,\frac{T_3}{T}\sqrt{0.40}} = 0.86\sqrt{\frac{T_3}{T}}$$

$$= 0.34\sqrt{\frac{1 + k_a}{(GB)_a T}} \tag{24}$$

at a bandwidth of

$$B_m = w_m/2\pi = \frac{1}{2\pi}\sqrt[4]{\frac{0.40}{0.58^2}\left(\frac{T}{T_3}\right)^2} = 0.166\sqrt{\frac{T}{T_3}}$$

$$= 0.42\sqrt{\frac{(GB)_a T}{1 + k_a}}. \tag{24a}$$

We note that DA_a decreases with increasing computing time T. The optimum computing time of a differential analyzer is therefore given by T_m, (17), the optimum computing time of the integrator. Replacing T by T_m in (24) we have

$$DA_{am} = 0.36\sqrt{\frac{(GB)_i}{(GB)_a}} = \frac{k_i\sqrt{1 + k_a}}{A_i}. \tag{25}$$

Comparison with DA_{im}, (18), yields

$$\frac{DA_{am}}{DA_{im}} = 0.90\sqrt{\frac{(1 + ka)(GB)_i}{(GB)_a}}. \tag{25a}$$

For best results, $(GB)_a$ should, therefore, be *larger* than $(GB)_i$. For $k_{a\max} = 3$, for example, $(GB)_a = 3(GB)_i$ equalizes the accuracies of integrators and adders at optimum integrator computing times.

Note that it is the GB product alone that matters for adders. For integrators on the other hand we have found that the gain itself should be high. A minimum gain exists only if the adder is to be directly calibrated: a fractional devation ϵ of its output from $-ke_i$ requires

$$A_a \geqq \frac{1 + k}{\epsilon}.$$

We regard an adder as isolated if it connects two branch points of a computing setup. A branch point is here to be understood as a point at which three or more computing elements connect. Frequently, however, adders are cascaded with integrators. Let us investigate this important case in some detail.

Integrator and Adder in Cascade

The combined transfer function is now

$$\overline{H} = \frac{1}{\left(p+\frac{T}{T_1}\right)\left(p+\frac{T}{T_2}\right)\left(p+\frac{T}{T_3}\right)} \propto \sim \frac{1}{\left(p+\frac{T}{T_1+T_3}\right)\left(p+\frac{T}{T_2}\right)},$$

where powers of p higher than the second have been neglected in the denominator. We have

$$T_1 = T_i/A_i; \qquad T_2 = A_iRC = TA_i/k_i \text{ with } k_i = T/RC;$$
$$T_3 = (1+k_a)T_a/A_a.$$

The subscripts i and a refer to integrator and adder, respectively, and T_i, $-A_i$ and T_a, $-A_a$ are the amplifier time-constants and gains. These results show that T_1 and T_3 play similar roles. The optimum computing time of the combination is greater than that of the isolated integrator, T_m (17); this follows at once from (13). The best time for a complete setup will, however, be taken as T_m, since there is likely to be at least one isolated integrator present and we have seen already that T must not be larger than T_m, whereas somewhat smaller times are of no consequence. Choosing $T=T_m$ and replacing T_1 in (13) by T_1+T_3 we obtain from (13), (17), and (18) after some algebra,

$$DA^2 = \frac{1}{6}\left(\frac{k_i}{A_i}\right)^2\left[1+\frac{k_a+1}{2}\frac{(GB)_i}{(GB)_a}\right] = DA_{im}{}^2\left[1+\frac{k_a+1}{2}\frac{(GB)_i}{(GB)_a}\right]. \tag{26}$$

Since $k=k_ak_i$ is fixed, best results are achieved if $(GB)_a$ is several times as large as $(GB)_i$; this allows us to work with high k_a and corresponding low k_i. Note also the possibility of obtaining high accuracy in integrators of comparatively low amplifier gain. Cascading an integrator with an adder allows us to reduce k_i; high accuracy results, provided $(GB)_a$ is sufficiently large.

Elements with *RC*-Coupled Amplifiers

As a more complicated application consider a computing element based on an amplifier with capacitive interstage coupling such as is used occasionally in repetitive computers. We shall neglect the effect of grid current and thus partially invalidate our results. In an actual example grid current would have to be considered separately.

Let T_c denote the time-constant introduced into the amplifier response by the coupling networks. It is shown in Appendix III that integrator performance is not substantially affected by $T<T_c$. For an adder (Appendix III)

$$\overline{H}(p) \propto \sim \frac{p}{\left(p+\frac{T}{T_3}\right)\left(p+\frac{T}{T_4}\right)} \propto \frac{1/T_3}{p+\frac{T}{T_3}} - \frac{1/T_4}{p+\frac{T}{T_4}} \tag{27}$$

where

$$T_a \triangleq \frac{1+k_a}{A}T_a; \qquad T_4 \triangleq \frac{A}{1+k_a}T_c; \quad T_4 \gg T_3. \tag{27a}$$

Therefore, (Fig. 8)

$$W(\tau) \propto \left[\frac{1}{T_3}\epsilon^{-(T/T_3)\tau} - \frac{1}{T_4}\epsilon^{-(T/T_4)\tau}\right]1(\tau). \tag{28}$$

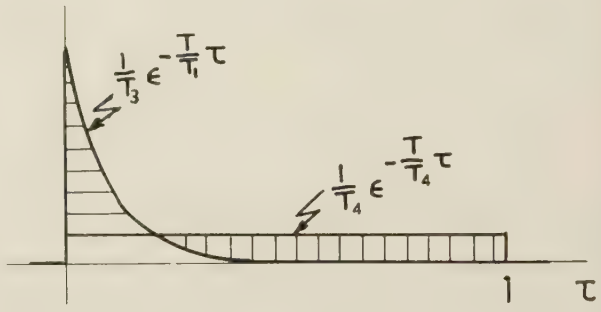


Fig. 8—Illustrating the memory function of the *RC*-coupled adder.

In addition to the ordinary error of adders, caused by the nonvanishing rise-time T_a of the amplifier, we notice an approximate integration due to the finite time-constant T_c of its interstage coupling networks. Under suitable restrictive assumptions, (Appendix V)

$$\epsilon_1{}^2 \cong \frac{1}{3}w_m{}^2\left(\frac{T_3}{T}\right)^2 + \frac{\pi}{w_m}\left(\frac{T}{T_4}\right)^2 \tag{29}$$

The first term will be recognized as the squared error of the direct-coupled adder, (23). The second term expresses the blocking of direct current. We now add $\epsilon_1{}^2$ and $\epsilon_2{}^2$, (9a), and obtain the square of the total error $\epsilon^2{}_{\text{tot}}$.

How does the additional term in $\epsilon_1{}^2$ affect the minimum of $\epsilon_{\text{tot}}{}^2$ with respect to w_m? It increases it and shifts it to the right. In order to obtain approximate results, we can, therefore, neglect $\epsilon_2{}^2$. The minimum of $\epsilon_1{}^2$ with respect to w_m then gives

$$DA \cong \epsilon_{1\min} \cong 1.6\frac{1+k}{A}\sqrt[3]{\frac{TT_a}{T_c{}^2}}. \tag{30}$$

As the results for ordinary integrators remain valid we now have all the fundamental relations required for the

design of RC-coupled computing elements. Further consideration of this problem would lead us too far astray from the main objects of our paper.

Single-Frequency Performance

We shall now investigate the performance of integrators and of adders with steady state sine inputs. It will be shown that the corresponding errors are usually comparatively small so that the use of wide-band considerations alone is then justified for our purposes. The fractional error was given in (3) as the phase difference between $\overline{H}_I$ and $\overline{H}_N$, the ideal and actual transfer functions of the computing element.

For an integrator with transfer function $\overline{H}_N$ of (11)

$$\sphericalangle \overline{H}_N \cong \operatorname{arc\,cot} \frac{w^2 - ab}{aw}, \qquad a \gg b;$$

$$\sphericalangle \overline{H}_I = -\pi/2$$

and, therefore

$$e_s \cong \Delta\phi \cong \left| \frac{w^2 - ab}{aw} \right| = \left| \frac{w^2 - \dfrac{T^2}{T_1 T_2}}{\dfrac{T}{T_1} w} \right|. \tag{31}$$

Subscript s refers to single frequency performance. This error is zero for

$$w = w_0 = T/\sqrt{T_1 T_2}. \tag{32}$$

At the optimum computing time of an integrator $T = T_m$, (17), and

$$w_0 = w_{0m} = 2.45\sqrt{A_i/k_i}. \tag{32a}$$

Let us find the frequency range for which $DA_s < DA_m$, maintaining the condition $T = T_m$. For high frequencies, $w \gg w_{0m}$,

$$e_i = e_i' \cong \frac{1}{6}\left(\frac{k_i}{A_i}\right)^2 w.$$

For low frequencies, $w \ll w_{0m}$,

$$e_i = e_i'' \cong \left(\frac{k_i}{A_i}\right) w.$$

Comparison with DA_m of (18) yields the result

$$e_i > DA_m, \text{ provided } 2.5 < w\, 2.5(A/k). \tag{33}$$

The lower limit cannot worry us; operation at frequencies below $w = 2.5$ is better evaluated by our wide-band methods. The upper limit is high enough to be quite safe.

For adders at $T = T_m$, using (3), (17), and (22)

$$e_a \cong w < T_a/T. \tag{34}$$

Comparison with DA_a, (25), results in

$$\frac{e_a}{DA_a} = 0.48w\sqrt{1 + k_a}\sqrt{\frac{(GB)_i}{(GB)_a}}\,\frac{k_i}{A_i} \text{ at } T = T_m. \tag{35}$$

For all reasonable values of w, $e_a < DA_a$ and it follows again that wide-band considerations furnish better criteria of performance.

There are, however, exceptions. For integrators, for example, it can be desirable to work at very high values of external gain k_i when inputs with a strongly dominating single frequency are to be integrated. This is due to the fact that integration of a steady state sine input of angular frequency w (in τ) and *amplitude* gain k' requires $k_i = wk'$. The upper bound in the provision of (33) then becomes $w < 1.6\sqrt{A_i/k'}$; if this restriction be overstepped, e_i should be considered.

Drift

The consideration of drift is outside the scope of this paper. Drift will of course influence the choice of design parameters. We shall confine ourselves to one remark. Let e_{id} be the input offset voltage required to compensate for output drift of an integrator. The output voltage due to drift, at the end of the computing interval T, is then Te_{id}, where e_{id} is assumed to be essentially constant. It is well to be aware of the fact that in integrators it is this quantity that matters rather than e_{id} itself.

Conclusion

We have developed a formalism sufficient for a systematic evaluation of the performance of linear computing elements using the effective error and some new concepts such as the computing bandwidth and the computing transfer function and introducing a quantitative definition of dynamic accuracy. Practical applications always deal with small errors and actual calculations can, therefore, be considerably simplified through suitable approximations.

Although dynamic accuracies have been calculated, only a few conclusions were drawn in this paper about the choice of parameters of design. The important question of the requirements for the best elements within the limitations of existing components were not touched; it is hoped to cover this topic in a further paper. Another question of interest would be the establishment of experimental techniques for the determination of DA and of computing bandwidth as here defined.

Appendix I

The Effect of Change of Scale on Output and on Transfer Function

On the new time scale τ, output is given in terms of input and impulse response by

$$e_0(\tau) = \int_0^\tau e_i(x) W(\tau - x)\, dx,$$

and on the old scale $t = T\tau$ by

$$e_{0t}(t) = e_{0t}(T\tau) = \int_0^{T\tau} e_{it}(x)W_t(T\tau - x)dx$$
$$= \int_0^{T\tau} e_i\left(\frac{x}{T}\right)\frac{1}{T}\,W\left(\tau - \frac{x}{T}\right)dx$$
$$= \int_0^{\tau} e_i(y)W(\tau - y)dy = e_0(\tau)$$

which proves the first relation. For the transfer function,

$$\overline{H}_t(p) = \int_0^{\infty} W_t(t)\epsilon^{-pt}dt$$

and

$$\overline{H}(p) = \int_0^{\infty} W(\tau)\epsilon^{-p\tau}d\tau = \int_0^{\infty} TW_t(T\tau)\epsilon^{-p\tau}d\tau$$
$$= \int_0^{\infty} W_t(t)\epsilon^{-(p/T)t}dt = \overline{H}_t\left(\frac{p}{T}\right)$$

as stated.

Appendix II

Proof of the Relation between Ordinary and Computing Transfer Functions

Transforming (4) we obtain

$$\overline{C} = \int_0^1 W(\tau)\epsilon^{-p\tau}d\tau = \int_0^{\infty} - \int_1^{\infty}$$
$$= \overline{H} - \int_1^{\infty} W(\tau)\epsilon^{-p\tau}d\tau$$
$$= \overline{H} - \epsilon^{-p}\int_0^{\infty} W(\tau + 1)\epsilon^{-p\tau}d\tau$$
$$= \overline{H} - \epsilon^{-p}[\overline{W(\tau + 1)1/\tau}],$$

which is (5).

Appendix III

Derivation of Transfer Functions

Consider the computing element of Fig. 9. $\overline{Z}_i$ and $\overline{Z}_f$ are the input and feedback impedances; $-A\overline{H}_a(p)$ is the transfer function of the amplifier, where $\overline{H}_a(0) = 1$ and $A \gg 1$.

The transfer function of the element is

$$\overline{H}_t(p) = -\frac{\overline{Z}_f}{\overline{Z}_i}\cdot\frac{1}{1 + \dfrac{1}{A\overline{H}_a(p)}\left[1 + \dfrac{\overline{Z}_f}{\overline{Z}_i}\right]}. \quad (36)$$

The Integrator

We take for the amplifier transfer function

$$\overline{H}_a = \frac{1}{1 + pT_a}.$$

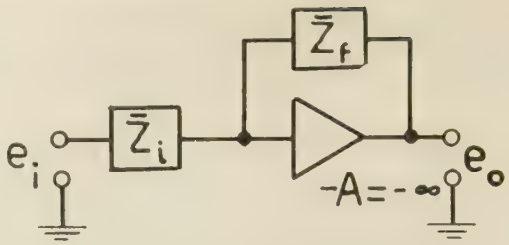


Fig. 9—Block diagram of a computing element.

Moreover

$$\overline{Z}_i = R; \qquad Z_f = \frac{1}{pC}; \qquad k_i \triangleq \frac{T}{RC};$$

and thus

$$\overline{H}_t(p) \cong -\frac{k_i}{T}\,\frac{1}{\left(p + \dfrac{1}{T_2}\right)(T_1p + 1)}, \quad (37)$$

where the time constants are

$$T_1 = \frac{T_a}{A_i}; \quad T_2 = A_iRC = \frac{A_i}{k_i}T. \quad (37a)$$

The Adder

With $\overline{H}_a$ as in above and

$$\overline{Z}_i = R_i; \qquad \overline{Z}_f = R_f; \qquad k_a \triangleq \frac{R_f}{R};$$

we obtain

$$\overline{H}_t = -\frac{k_a}{1 + pT_3}; \quad (38)$$

with a time constant

$$T_3 = \frac{1 + k_a}{A_a}T_a. \quad (38a)$$

The RC-Coupled Integrator

Now

$$Z_i = R; \qquad \overline{Z}_c = \frac{1}{RC}; \qquad k_i \triangleq \frac{T}{RC};$$

but

$$\overline{H}_a = \frac{p}{(pT_a + 1)\left(p + \dfrac{1}{T_c}\right)}; \qquad T_c \gg T_a.$$

T_c is the large time constant of the capacitive interstage coupling networks of the amplifier. It follows

$$\overline{H}_t \cong -\frac{1}{RC}\cdot\frac{p}{\dfrac{T_a}{A_i}p^3 + p^2 + \dfrac{1}{A_iRC}p + \dfrac{1}{A_iRCT_c}},$$

provided $A_iRC \gg T_c$. (39)

For high frequencies; *i.e.*, small t, we neglect the last term in the denomimator. The result is then identical with that for the direct coupled integrator, (37). For low frequencies, or large t, we neglect the first term in the denominator and

$$\overline{H}_t \cong -\frac{1}{RC}\frac{p}{\left(p+\frac{1}{2A_iRC}\right)^2+\omega_p{}^2}; \quad \omega_p{}^2 \triangleq \frac{1}{A_iRCT_c};$$

$t \gg 0.$

Thus

$$W(t) \cong -\frac{1}{RC}\epsilon^{-t/A_iRC}\cos\omega_p t\mathbf{1}(t)$$

$$\cong -\frac{1}{RC}\left(1-\frac{t}{2A_iRC}-\frac{t^2}{2A_iRCT_c}\right)\mathbf{1}(t), \; t \ll \sqrt{A_iRCT_c};$$

$t \gg 0.$

Combining these results we obtain without restriction on t

$$W(t) \cong -\frac{1}{RC}\left[1-\epsilon^{-t/T_1}-\frac{t}{2A_iRC}-\frac{t^2}{2A_iRCT_c}\right]\mathbf{1}(t);$$

$$t \ll \sqrt{A_iRCT_c}. \tag{39a}$$

It follows that the effect of the coupling term is negligible as long as the computing time T is smaller than T_c, the coupling time constant.

The RC-Coupled Adder

$$\overline{Z}_i = R_i; \qquad \overline{Z}_f = R_f; \qquad k_a \triangleq \frac{R_f}{R_i}$$

as for the direct-coupled adder and $\overline{H}_a$ as in the last Section.

$$\overline{H}_t(p) \propto -\frac{p}{p^2+p\left[\frac{A_a}{1+k_a}\frac{1}{T_a}+\frac{1}{T_a}+\frac{1}{T_c}\right]+\frac{1}{T_aT_c}}$$

$$\cong -\frac{p}{\left(p+\frac{1}{T_3}\right)\left(p+\frac{1}{T_4}\right)}, \tag{40}$$

where

$$T_3 = \frac{1+k_a}{A_a}T_a; \qquad T_4 = \frac{A_a}{1+k_a}T_c.$$

Appendix IV

Determination of Integrator *DA*

For an integrator we can write (2b), using $C_I = \mathbf{1}(\tau)\mathbf{1}(1-\tau)$,

$$\epsilon^{\infty 2} = DA_i{}^2 = \frac{\widetilde{(c_N - \widetilde{c_N})^2}}{\widetilde{c_N{}^2}}$$

where the wriggles indicate averages. Now $a \gg b$ and we shall also assume $ab \gg 1$; *i.e.*,

$$\frac{A_iT}{T_a}\frac{k_i}{A_i} \gg 1 \quad \text{or} \quad T \gg \frac{T_a}{k_i}.$$

Therefore

$$\widetilde{c_N} = \int_0^1 (\epsilon^{-b\tau}-\epsilon^{-a\tau})d\tau = \frac{\epsilon^{-a}-1}{a}-\frac{\epsilon^{-b}-1}{b}$$

$$\cong 1-\frac{1}{a}-\frac{b}{2};$$

$$\widetilde{c_N{}^2} \cong 1-\frac{2}{a}-b \cong 1;$$

$$\widetilde{(c_N-\widetilde{c_N})^2} \cong \int_0^1 \left(e^{-b\tau}-\epsilon^{-a\tau}-1+\frac{1}{a}+\frac{b}{2}\right)^2 d\tau$$

$$\cong \frac{1}{2a}+\frac{1}{12}b^2+\frac{b}{a}-\frac{1}{a^2} \cong \frac{1}{2a}+\frac{1}{12}b^2,$$

and

$$DA_i{}^2 \cong \frac{6+ab^2}{12a}$$

which is (13).

Appendix V

Calculation of Accuracy of the *RC*-Coupled Adder

We shall use a short cut in order to avoid the lengthy direct calculation. Eq. (28) consists of two terms. The first will be recognized as the impulse response of the direct coupled adder. The second term is approximately equal to $(1/T_4)(\tau)\mathbf{1}$; it represents, therefore, the impulse response of integration. Neglecting the small interaction between both terms we take over (23) for the error caused by the first term; *i.e.*,

$$\epsilon_{11}{}^2 = \frac{1}{3}w_m{}^2\left(\frac{T_3}{T}\right)^2.$$

The second term causes nothing but an error output; it corresponds to a computing transfer function

$$\overline{C} = -\frac{1}{jw}\frac{T}{T_4}(1-\epsilon^{-jw}),$$

or

$$|\overline{C}|^2 = \frac{2}{w^2}\left(\frac{T}{T_4}\right)^2(1-\cos w).$$

Our standard input is given by

$$|\bar{e}_i| = \mathbf{1}(w)\mathbf{1}(w - w_m).$$

The normalized output is the second error term and we have

$$\epsilon_{12}^2 = \frac{1}{w_m}\int_0^{w_m} |\bar{C}_i|^2 dw = \frac{2}{w_m}\left(\frac{T}{T_4}\right)^2 \int_0^{w_m} \frac{1-\cos w}{w^2}\, dw$$

$$\cong \frac{\pi}{w_m}\left(\frac{T}{T_4}\right)^2, \qquad \text{provided } w_m \gg 1.$$

Adding both terms,

$$\epsilon_1^2 = \frac{1}{3} w_m^2 \left(\frac{T_3}{T}\right)^2 + \frac{\pi}{w_m}\left(\frac{T}{T_4}\right)^2.$$

The integral can be calculated by contour integration. The salient steps follow.

$$\int_0^{w_m} = \int_0^{\infty} - \int_{w_m}^{\infty}; \quad \int_0^{\infty} \frac{1-\cos w}{w^2}\, dw$$

$$= \frac{1}{2}\int_{-\infty\to\infty} \frac{1-\epsilon^{jz}}{z^2}\, dz = \frac{1}{2}\cdot\frac{1}{2}\cdot 2\pi j \operatorname{Res}\left\{\frac{1-\epsilon^{jz}}{z^2}\right\}$$

$$= \frac{\pi}{2}.$$

For

$$w_m \gg 1, \qquad \int_{w_m}^{\infty} \frac{1-\cos w}{w^2}\, dw \cong \int_{w_m}^{\infty} \frac{dw}{w^2} = \frac{1}{w_m}.$$

Thus

$$\int_0^{w_m} \frac{1-\cos w}{w^2}\, dw \cong \frac{\pi}{2} - \frac{1}{w_m} \cong \frac{\pi}{2}.$$

Trigonometric Resolution in Analog Computers by Means of Multiplier Elements*

R. M. HOWE† AND E. G. GILBERT

Summary—**A method of generating sine and cosine functions in analog computers by means of multiplier elements and integrators is discussed. Static accuracy of the method is analyzed and found to be essentially equal to the accuracy of the multipliers employed. The system accepts $d\theta/dt$ as the input and generates output voltages of sin θ and cos θ. Amplitude-stabilizing loops are employed to maintain $\sin^2\theta+\cos^2\theta=1$. Advantages of the method include representation of unlimited range in angles, dynamic capabilities far beyond that of the multipliers alone, and possibility of employing electronic multipliers. The method has been successfully used to compute Euler angles in analog computer solutions of the three-dimensional flight equations.**

Introduction

MANY of the problems solved by analog computers require the generation of trigonometric functions. For example, in solving the three-dimensional flight equations, the Euler-angle computation requires generation of sine and cosine functions of the Euler angles. In present general-purpose electronic differential analyzers this is usually accomplished by servo-driven sine-cosine potentiometers or by diode function generators.

The purpose of this paper is to describe an alternative method of generating sine and cosine functions which involves only multipliers as nonlinear elements. Furthermore, this new method allows continuous angular travel through an indefinite number of revolutions, whether servo or all-electronic multipliers are used.

This resolving method has been discovered independently by other groups, but to our knowledge has not previously been published nor analyzed completely with regard to static and dynamic accuracy.[1]

Description of the New Resolving Technique

The new resolving technique is based on the solution of the equation

$$\frac{d^2x}{d\theta^2} + x = 0 \tag{1}$$

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[1] Similar self-correcting methods are described for stabilization of harmonic oscillators and for direction-cosine computation in the following notes issued by the University of Chicago, Advisory Board on Simulation:

M. D. Clement, "A Stabilized Harmonic Oscillator," IN-21, December 10, 1954.

J. P. Corbett, "Orthogonalizing and Normalizing Corrections for Direction Cosine Computation by Differential Analyzers," TN 54, December 2, 1954.

This method has also been used by the Analog Computer Section, Aero. Res. Labs., Wright Air Dev. Ctr.

with initial conditions

$$x(0) = 0, \qquad \frac{dx}{d\theta}(0) = 1. \tag{2}$$

The solution to (1) with the conditions in (2) is simply

$$x = \sin\theta \tag{3}$$

$$y = \frac{dx}{d\theta} = \cos\theta \tag{4}$$

which can then be used to provide coordinate resolutions involving the angle θ.

In (1) the independent variable is θ, whereas the electronic differential analyzer (electronic analog computer) can integrate only with respect to time t. But by multiplying the integrand by $d\theta/dt$ before integrating, the integration with respect to θ is effectively accomplished. Thus

$$\int z\left(\frac{d\theta}{dt}\right)dt = \int z\,d\theta. \tag{5}$$

The electronic differential analyzer circuit for accomplishing the solution to (1) is shown in Fig. 1. Note that the input to each integrator is multiplied by $d\theta/dt$ (*i.e.*, $\dot{\theta}$) before being integrated with respect to time. The multipliers shown schematically in the circuit could be either servo or all-electronic.

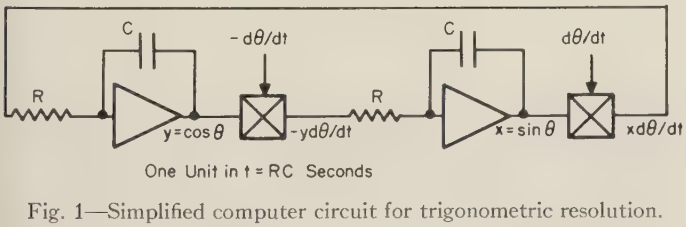

Fig. 1—Simplified computer circuit for trigonometric resolution.

One difficulty with the circuit as it is shown in Fig. 1 is the tendency of the solution to drift so that $\cos^2\theta+\sin^2\theta \neq 1$. For example, if $\dot{\theta}=\omega=$constant, the theoretical solution would be $x=\sin\omega t$, $y=\cos\omega t$. Due to power loss in the feedback capacitors the solution may damp somewhat. The net result is that after several cycles x^2+y^2 is no longer unity, but perhaps a per cent too low. Other computer errors such as dynamic multiplier errors, integrator drifts, etc., can cause similar errors.

This error in amplitude can be calculated using multipliers and a summer to obtain $1-(x^2+y^2)$. Thus define the error ϵ by

$$\epsilon = 1 - (x^2 + y^2). \tag{6}$$

The magnitude of x and y can be adjusted automatically upward or downward as needed by providing each integrator with negative or positive damping proportional to ϵ. This is shown in Fig. 2 where ϵ is computed by (6) above, multiplied by x and y, and fed back into integrators 2 and 1, respectively.

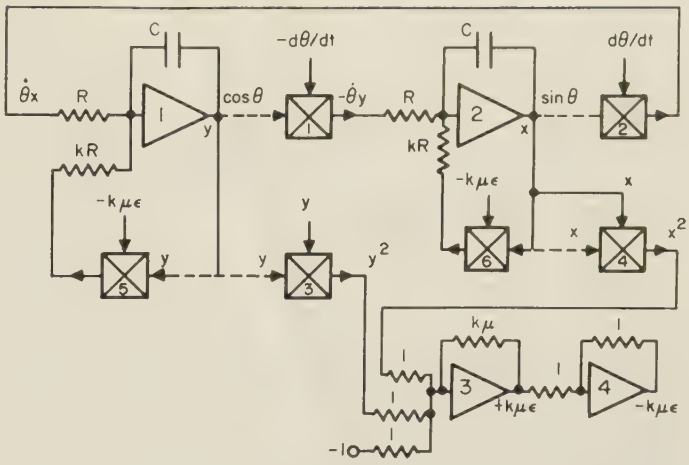

Fig. 2—Complete computer circuit for trigonometric resolution.

When servo-driven potentiometers are used for multiplication, this resolving circuit requires two servos, each with at least 3 multiplying potentiometers in addition to the reference potentiometer. The shaft angle of each servo is proportional to $\cos\theta$ and $\sin\theta$, respectively. This means that additional ganged potentiometers on each shaft can be used to multiply $\cos\theta$ or $\sin\theta$ by other voltages. The output voltages of integrators 1 and 2 are also proportional to $\cos\theta$ and $\sin\theta$, respectively.

If all-electronic multipliers of the time-division type are used, two masters (one for $\cos\theta$, one for $\sin\theta$) are needed, with 3 slaves for each master. Additional slaves can be used to multiply $\cos\theta$ or $\sin\theta$ by other voltages.

To summarize, the resolving method described here accepts $+\theta$ and $-\theta$ voltages as inputs, providing output voltages and shaft angles (or master pulses) proportional to $\cos\theta$ and $\sin\theta$. The over-all requirement is two multipliers, each with three channels, two integrating amplifiers, and four summing amplifiers.

In the next section the static and dynamic accuracy of this resolving technique is analyzed. It will be shown that servo multiplers are to be preferred over electronic multipliers if the servo bandwidth is adequate.

Static and Dynamic Accuracy Analysis of the Resolving Technique

In this section a detailed study is made of the factors influencing resolver accuracy. It is shown that static accuracy is as good as the multiplier static accuracy, while dynamic accuracy is generally better than the multiplier dynamic accuracy. Exact solution of the resolver equation is important and will be developed first.

Exact Solution of the Resolver Equations

It is convenient to write the second order resolver equation solved in Fig. 2 as two first order equations. Letting the first and second integrator outputs be y and x, respectively, one obtains

$$\frac{dx}{dt} = \frac{d\theta}{dt}\,y - \mu(x^2 + y^2 - 1)x \tag{7}$$

and

$$\frac{dy}{dt} = -\frac{d\theta}{dt}\,x - \mu(x^2 + y^2 - 1)y. \tag{8}$$

The analytic solution for these equations is best obtained by expressing x and y in polar form. Thus define the polar variables R and ϕ by

$$x = R\sin\phi \tag{9}$$

$$y = R\cos\phi. \tag{10}$$

In terms of R and ϕ perfect resolution is obtained when $R=1$ and $\theta=\phi$. Substituting (9) and (10) into (7) and (8) gives

$$R\frac{d\phi}{dt}\cos\phi + \frac{dR}{dt}\sin\phi = \frac{d\theta}{dt}R\cos\phi - \mu(R^2-1)R\sin\phi \tag{11}$$

$$-R\frac{d\phi}{dt}\sin\phi + \frac{dR}{dt}\cos\phi = -\frac{d\theta}{dt}R\sin\phi - \mu(R^2-1)R\cos\phi. \tag{12}$$

Eqs. (11) and (12) can be written as single equations in R and ϕ in the following way. Multiply (11) by $\sin\phi$ and (12) by $\cos\phi$ and add, obtaining

$$\frac{dR}{dt} = -\mu(R^2-1)R. \tag{13}$$

Similarly, multiply (11) by $\cos\phi$ and (12) by $\sin\phi$ and subtract, getting

$$\frac{d\phi}{dt} = \frac{d\theta}{dt}, \quad \text{or} \quad \phi = \theta + \phi(0). \tag{14}$$

Eq. (14) implies that if (11) and (12) are solved exactly with ideal computer components, as indicated in Fig. 2, then $\phi=\theta$ as required, unless the initial value of ϕ is in error by $\phi(0)$. But this possibility of error is present also in a conventional resolver if $d\theta/dt$ is integrated directly to obtain θ.

To study the behavior of (13) it is convenient to introduce the variable r, which is the deviation of R from unity. Thus let

$$r = R - 1. \tag{15}$$

Eq. (13) then becomes

$$\frac{dr}{dt} = -\mu(1+r)(2+r)r. \tag{16}$$

In the usual case $r \ll 1$ and (16) reduces to

$$\frac{dr}{dt} = -2\mu r, \qquad r \ll 1. \tag{17}$$

For an initial error in x^2+y^2, *i.e.*, for $R(0)\neq 1$, r has an initial value r_0, and the solution to (17) is simply

$$r = r_0 e^{-2\mu t}. \tag{18}$$

Thus the error in R decays exponentially to zero with a time constant $1/(2\mu)$. This time constant can be reduced by making the correction gain-factor μ large.

Up to now, then, we have shown that accurate resolution is obtained when ideal computing elements are used, despite any integrator initial-condition errors. At worst the error in angle is simply a constant $\phi(0)$ equal to the initial angular error caused by incorrect integrator initial conditions, while the error r in magnitude decays rapidly to zero. In the following sections the errors in resolving due to both static and dynamic errors in the computing components will be analyzed.

Errors Due to Static Inaccuracies in Components

The static errors in computing components take the form of zero offsets, nonlinearities, and gain inaccuracies. To implement the following analysis, such component errors must be defined in mathematical terms. For a multiplier whose inputs are x and y one may write

$$\text{multiplier output} = xy + E(x, y) \tag{19}$$

where xy is the desired product and $E(x, y)$ an error term. If a servomultiplier is used and x is the shaft quantity, y does not contribute directly to the error and

$$E(x, y) = yP(x). \tag{20}$$

$P(x)$ is an error function dependent on servoshaft position error and potentiometer nonlinearity. The servomultiplier possesses, therefore, a zero point error advantage in that $E(x, 0)=0$. Integrator errors, primarily due to amplifier unbalance and grid current, may be represented by an equivalent voltage I which appears at the integrator input. Integrator gain errors, summing amplifier gain errors, and summing amplifier offsets are relatively minor and may be included in the error analysis of Fig. 2 as part of the multiplier errors.

The component errors as just described may now be introduced into (7) and (8). Subscripts on the quantities E, P, and I refer to the component numbers in Fig. 2. After making the necessary substitutions and transformations (see Appendix), one obtains

$$R - 1 \cong r = -\tfrac{1}{2}\left[E_3(\cos\theta, \cos\theta) + E_4(\sin\theta, \sin\theta)\right] \tag{21}$$

$$\dot{\phi} \cong \dot{\theta} - \cos\theta\left[E_1(\cos\theta, -\dot{\theta}) + \frac{1}{k}E_6(\sin\theta, 0) + I_2\right] + \sin\theta\left[E_2(\sin\theta, \dot{\theta}) + \frac{1}{k}E_5(\cos\theta, 0) + I_1\right]. \tag{22}$$

These equations give the minimum static errors and hold if μ is made large by the inequality

$$\mu \gg \left| \frac{\left| E_1 + \frac{1}{k} E_6 + I_2 \right| + \left| E_2 + \frac{1}{k} E_5 + I_1 \right|}{\left| E_3 + E_4 \right|} \right|_{\max} \quad (23)$$

and θ varies slowly. Hence, the errors E_3 and E_4 in multipliers 3 and 4 affect only r and not ϕ, while the errors E_1, E_2, E_5, and E_6 in multipliers 1, 2, 5, and 6 affect only ϕ and not r. Note that the influence of E_5 and E_6 can be made smaller by making k as large as possible without causing amplifiers 3 and 4 to saturate. If the integrator errors I_1 and I_2 are negligible, a good assumption, it then becomes clear that the error in angular rate $\dot{\phi}$ of the resolver is the order of the errors E_1 and E_2 in multipliers 1 and 2. For many electronic multipliers this error may be the order of 0.1 per cent of full scale, even when $\dot{\theta}=0$. A drift rate in $\dot{\phi}$ of 0.1 per cent of maximum $\dot{\phi}$ would result, and this could be serious in certain applications.

On the other hand, if servomultipliers are used, we see from (20) that ϕ in (22) becomes

$$\dot{\phi} = \dot{\theta}[1 + P_1(\cos\theta)\cos\theta + P_2(\sin\theta)\sin\theta] - I_2\cos\theta + I_1\sin\theta. \quad (24)$$

Multiplier errors P_1 and P_2 are simply equivalent to errors in integrator gains, and when $\dot{\theta}=0$, the drift error in ϕ is the order of integrator drifts, which are normally quite small.

In summary it has been shown that static errors in the resolver outputs are minimized when μ is large as determined by (23) and servomultipliers are employed. Under these conditions the following statements apply:

1) When the outputs $x=\sin\theta$ and $y=\cos\theta$ are expressed with polar coordinates R and ϕ, where ideally $R=1$ and $\phi=\theta$, then the error r in the value of R is given by (21) and is approximately equal to the average error in multipliers 3 and 4.
2) Errors in the integration of θ are the same order as errors in multipliers 1 and 2.
3) Drifts in ϕ are at least as small as integrator drifts.
4) Errors in multipliers 5 and 6 are relatively unimportant.

Errors due to Potentiometer Granularity in Servomultipliers

Another type of static error is created by the step discontinuities in wire-wound potentiometers and is characteristic of both new and conventional resolving techniques which employ servo-driven potentiometers. Assume that one-turn potentiometers with a total of N turns of wire are used. In the conventional sine-cosine potentiometer method of resolving, a full revolution represents 2π radians, so that there are $N/2\pi$ turns of wire per radian. In the new resolving method a full multiplier potentiometer revolution represents a range in $\sin\theta$ or $\cos\theta$ from -1 to $+1$, *i.e.*, a total range of 2. Thus in the region where $\theta=0$ or π (the most critical regions for potentiometer granularity in computing $\sin\theta$) $\sin\theta\cong\theta$, and there are $N/2$ turns of wire per radian. Hence the effect of wire-wound potentiometer granularity is reduced by a factor of π when comparing new and conventional resolving techniques. This feature is important in obtaining the maximum smoothness of resolver output.

Dynamic Errors

In this section dynamic errors of the new resolving method are analyzed by considering sinusoidal response characteristics. Two general cases will be considered: 1) resolver performance when $d\theta/dt=$constant, so that ideally the resolver outputs are $\sin\omega t$ and $\cos\omega t$, where $\omega=\dot{\theta}$; 2) resolver performance when $\dot{\theta}=\omega\delta\cos\omega t$, where $\delta\ll 1$. Only servomultipliers will be considered.

First let us analyze the case where $\dot{\theta}=$constant. In the steady state it is clear that the outputs y and x of integrators 1 and 2 will be sinusoidal with constant amplitude. If both multiplier dynamics are the same, it is evident from symmetry that x and y will have the same steady-state amplitude R. For the sinusoidal outputs to remain constant it is also clear that the output of integrator 1 must lead the output of integrator 2 by $\pi/2$, so that total phase shift around the loop is π. Thus let

$$x = R\sin\omega t \quad (25)$$

$$y = R\cos\omega t \quad (26)$$

where the constants R and ω are to be determined.

Next let us assume that the output voltages of the multipliers can be described in terms of a magnitude M and a phase-shift N for sinusoidal inputs of magnitude R and frequency ω. M and N can either be calculated from previous information or can be measured experimentally. Thus the output of multiplier 1 can be written

$$\text{output of multiplier 1} = -R\dot{\theta}M\cos(\omega t + N). \quad (27)$$

In the same way

$$\text{output of multiplier 2} = R\dot{\theta}M\sin(\omega t + N). \quad (28)$$

Similarly,

$$\text{output of multiplier 3} = R^2M\cos\omega t\cos(\omega t + N) \quad (29)$$

and

$$\text{output of multiplier 4} = R^2M\sin\omega t\sin(\omega t + N). \quad (30)$$

Thus the output of amplifier 4 is given by

$$\text{output of amplifier 4} = k\mu\{R^2M[\sin\omega t\sin(\omega t + N) + \cos\omega t\cos(\omega t + N)] - 1\} = k\mu[R^2M\cos N - 1]. \quad (31)$$

This signal is fed through multiplier 5 to give

$$\text{output of multiplier 5} = k\mu MR(R^2M\cos N - 1)\cos(\omega t + N) \quad (32)$$

which, finally, is multiplied by $1/k$ and summed with the output of multiplier 2 to give the input to integrator 1. But from (26) the input to integrator 1 is also given by $\omega R \sin \omega t$. Hence from (28) and (32) we have

$$R\dot{\theta}M \sin (\omega t + N) + \mu MR(R^2M \cos N - 1) \cos (\omega t + N) = \omega R \sin \omega t$$

or

$$M\sqrt{\dot{\theta}^2 + \mu^2(R^2M \cos N - 1)^2} \sin (\omega t + N + \gamma) = \omega \sin \omega t \quad (33)$$

where

$$\tan \gamma = \frac{\mu(R^2M \cos N - 1)}{\dot{\theta}}. \quad (34)$$

Equating magnitudes and phase angles on both sides of (33), we obtain

$$R^2 = \frac{1}{M \cos N}\left(1 - \frac{\dot{\theta}}{\mu} \tan N\right) \quad (35)$$

and

$$\omega = \frac{M\dot{\theta}}{\cos N}. \quad (36)$$

For the case where the phase error N of the multiplier is small and where $N\dot{\theta}/\mu \ll 1$, it follows that

$$R \cong \frac{1}{\sqrt{M}}\left(1 - \frac{\dot{\theta}N}{2\mu}\right), \quad N \ll 1, \quad \frac{N\dot{\theta}}{\mu} \ll 1 \quad (37)$$

and

$$\omega \cong M\dot{\theta}. \quad (38)$$

The effect of the multiplier magnitude factor M and phase error N is now clear when $\dot{\theta}$ = constant; the magnitude of the resulting sinusoidal response is shifted slightly from unity in accordance with (37), while the angular frequency ω is in error by the factor $M-1$.

It is important to note that R in (37) is the magnitude of the sinusoidal output of integrators 1 and 2. If additional trigonometric multiplications are to be performed using extra pots on the shafts of servos 1 and 2, then the magnitude R_s of the sin ωt and cos ωt factors in the external trigonometric multiplications will be given by

$$R_s = MR = \frac{\left(1 - \frac{\dot{\theta}}{\mu} \tan N\right)^{1/2}}{(\cos N)^{1/2}} M^{1/2}. \quad (39)$$

For small N this reduces to

$$R_s = \left(1 - \frac{\dot{\theta}N}{2\mu}\right) M^{1/2}, \quad N \ll 1, \quad \frac{N\dot{\theta}}{\mu} \ll 1. \quad (40)$$

The phase shift will of course be N radians with respect to the integrator 1 and 2 outputs respectively.

As an example of the order of magnitude of errors involved, consider a servomultiplier with an undamped natural frequency of 100 radians/second ($\sim$16 cps) and let $\dot{\theta} = 3$ radians/second ($\sim$0.5 cps). Reasonable values for M and N under these conditions would be $M = 1.001$ and $N = 0.01$ radian. Assume that $\mu = 10$. From (40) the error in magnitude at the servoshafts will be 0.1 per cent while from (38) the error in frequency will be 0.1 per cent.

Next let us consider the dynamic errors in the resolver method when servos are used and the input angular rate $\dot{\theta}$ is a sinusoidal oscillation given by

$$\dot{\theta} = \delta\omega \cos \omega t \quad (41)$$

from which

$$\theta = \theta_0 + \delta \sin \omega t. \quad (42)$$

We will consider the case where $\delta \ll 1$, *i.e.*, where the angle θ consists of a small sinusoidal oscillation about a constant angle θ_0. This type of dynamic performance is often required in solving aircraft or missile flight equations.

It is difficult to solve this problem analytically for the general case where the multipliers have a magnitude M and phase shift N for each of the harmonic frequencies which will make up the steady-state resolver outputs x and y. However, of particular interest is the solution where $M = 0$, *i.e.*, where the frequency ω is so high that the servomultipliers cannot follow the outputs x and y at all. In this case the average output voltages x and y from integrators 2 and 1 in Fig. 2 will be sin θ_0 and cos θ_0 respectively, and the shaft angles of multipliers 1 and 2 will have constant displacements given by sin θ_0 and cos θ_0, respectively. Thus the input to integrator 2 will be $-\dot{\theta} \cos \theta_0 = -\delta\omega \cos \omega t \cos \theta_0$, from which the output x is given by

$$x = \sin \theta_0 + \delta \cos \theta_0 \sin \omega t. \quad (43)$$

Similarly, the input to integrator 1 is $\dot{\theta} \sin \theta_0 = \delta\omega \cos \omega t \sin \theta_0$, so that the output y is given by

$$y = \cos \theta_0 - \delta \sin \theta_0 \sin \omega t. \quad (44)$$

The outputs of a perfect resolver would be given from (42) by

$$x = \sin \theta = \sin (\theta_0 + \delta \sin \omega t) \quad (45)$$

$$y = \cos \theta = \cos (\theta_0 + \delta \sin \omega t). \quad (46)$$

Eq. (45) can be rewritten as

$$x = \sin \theta_0 \cos (\delta \sin \omega t) + \cos \theta_0 \sin (\delta \sin \omega t). \quad (47)$$

Expanding cos (δ sin ωt) and sin (δ sin ωt) in power series, we obtain

$$x = \sin \theta_0\left[1 - \frac{(\delta \sin \omega t)^2}{2} + \cdots\right] + \cos \theta_0\left[\delta \sin \omega t - \frac{(\delta \sin \omega t)^3}{3!} + \cdots\right]. \quad (48)$$

It is now clear that the resolver output x given by (43) when multiplier dynamic response is zero equals the zeroth and first order terms in the series representation for the ideal resolver, as given in (48). This means that the actual resolver output will be very nearly equal to the ideal output providing $\delta \ll 1$. Similarly, from (46)

$$y = \cos\theta_0\left[1 - \frac{(\delta \sin \omega t)^2}{2} + \cdots\right] - \sin\theta_0\left[\delta \sin \omega t - \frac{(\delta \sin \omega t)^3}{3!} + \cdots\right] \quad (49)$$

which shows that the actual resolver output y given in (44) represents the first two terms of the ideal resolver output.

To summarize, if the angle θ consists of a constant θ_0 plus a small-amplitude sinusoidal oscillation, the resolving method gives accurate sin θ and cos θ outputs even when the frequency ω is so high that the servo-multipliers have no response at all at that frequency. Unless rather severe resonant peaks are present in the servos, it seems reasonable to assume that at lower frequencies the results would be somewhat better. Note that these conclusions apply to the voltages x and y appearing at the integrator outputs. The servoshaft motion will not be accurate at all, and electronic multipliers would need to be used to multiply x and y by other voltages, as required in the particular problem.

This suggests the possibility of employing servo-multipliers for the resolving method because of drift considerations, but still using electronic multipliers for further required multiplications by the resolver outputs $x = \sin\theta$ and $y = \cos\theta$.

One disadvantage of this resolving technique is the requirement of the time derivative $d\theta/dt$ of the angle as an input voltage. However, in many cases $d\theta/dt$ is readily available because of the problem mechanization. For example, this is true in computing the sines and cosines of the Euler angles, as needed in a three-dimensional flight simulation.

Rectilinear to Polar Resolution

Thus far we have described how to use the new resolving method to produce sin θ and cos θ, given $d\theta/dt$. Actually, this is the polar to rectilinear conversion problem, *i.e.*, given θ and R, compute $a = R\cos\theta$ and $b = R\sin\theta$. An equally important problem is to calculate θ and R, given a and b, *i.e.*, the rectilinear to polar conversion problem. This can be accomplished by recognizing that

$$\frac{b}{a} = \tan\theta = \frac{\sin\theta}{\cos\theta} \text{ or } b\cos\theta - a\sin\theta = 0.$$

Using the new resolving method $b\cos\theta - a\sin\theta$ is computed. This will in general not be zero because θ will not have its proper value. The resulting nonzero signal is amplified and fed into the $d\theta/dt$ inputs to the resolver, so that the sin θ and cos θ outputs are driven to the appropriate values representing the correct θ.[2] By integrating $d\theta/dt$ at the same time, the voltage θ is obtained. R is calculated from the formula

$$R = a\cos\theta + b\sin\theta.$$

If R varies over wide limits in any particular problem, it will be necessary to use an automatic gain control in the $d\theta/dt$ input to make the loop gain proportional to $1/R$.

This method of rectilinear to polar conversion has several disadvantages. The angle θ (a voltage) and the functions sin θ and cos θ are self-consistent only if the integrator which produces θ from $\dot\theta$ is perfect. As a result, integrator drift and gain error limit the time of accurate computation. Furthermore, the angular range of θ is restricted by amplifier saturation. The more conventional servo resolver which has a shaft angle θ does not possess these limitations.

Appendix

Static Error Equations

Introduction of error functions in (7) and (8) gives

$$\dot x = \dot\theta y - \mu(x^2 + y^2 - 1)x - E_1(y, -\dot\theta) - \mu[E_3(y, y) + E_4(x, x)]x - \frac{1}{k}E_6(x, -k\mu\bar\epsilon) - I_2 \quad (50)$$

$$\dot y = -\dot\theta x - \mu(x^2 + y^2 - 1)y - E_2(x, \dot\theta) - \mu[E_3(y,y) + E_4(x,x)]y - \frac{1}{k}E_5(y, -k\mu\bar\epsilon) - I_1 \quad (51)$$

where $k\mu\bar\epsilon$ is now the output of amplifier 3 or

$$\bar\epsilon = 1 - (x^2 + y^2) - E_3 - E_4. \quad (52)$$

These equations are next converted to polar form according to (9) and (10) and the following expressions for $\dot R$ and $\dot\phi$ are obtained in the same manner as (13) and (14) were obtained.

$$\dot R = -\mu(R^2 - 1)R - \mu R[E_3 + E_4] - \sin\phi\left[E_1 + \frac{1}{k}E_6 + I_2\right] - \cos\phi\left[E_2 + \frac{1}{k}E_5 + I_1\right] \quad (53)$$

$$\dot\phi = \dot\theta - \frac{\cos\phi}{R}\left[E_1 + \frac{1}{k}E_6 + I_2\right] + \frac{\sin\phi}{R}\left[E_2 + \frac{1}{k}E_5 + I_1\right] \quad (54)$$

[2] The amount of amplification in the $d\theta/dt$ input will determine the time constant of the corrective action.

with

$$\bar{\epsilon} = 1 - R^2 - E_3 - E_4. \tag{55}$$

If the resolver errors are small, $r \ll 1$ and $\phi \cong \theta$ which allows (53)-(55) to be simplified to

$$\frac{1}{2\mu}\dot{r} + r = -\frac{1}{2}[E_3 + E_4] - \frac{\sin\theta}{2\mu}\left[E_1 + \frac{1}{k}E_6 + I_2\right] - \frac{\cos\theta}{2\mu}\left[E_2 + \frac{1}{k}E_5 + I_1\right] \tag{56}$$

$$\dot{\phi} = \dot{\theta} - \cos\theta\left[E_1 + \frac{1}{k}E_6 + I_2\right] + \sin\theta\left[E_2 + \frac{1}{k}E_5 + I_1\right] \tag{57}$$

$$\bar{\epsilon} = -2r - E_3 - E_4. \tag{58}$$

Eq. (56) shows that increases in μ will effect decreases in r until μ is so large that

$$|E_3 + E_4| \gg \frac{1}{\mu}\left|E_1 + \frac{1}{k}E_6 + I_2\right| + \frac{1}{\mu}\left|E_2 + \frac{1}{k}E_5 + I_1\right|. \tag{59}$$

Thus a minimum error r is obtained when (59) is satisfied and is given by

$$r \cong -\tfrac{1}{2}[E_3(\cos\theta, \cos\theta) + E_4(\sin\theta, \sin\theta)] \tag{60}$$

provided θ varies slowly enough for $\dot{r}/2\mu$ to be small compared to r. Note that large μ makes $\bar{\epsilon} \cong 0$, a condition which might be expected from the nature of the feedback loops. Under the same conditions

$$\dot{\phi} \cong \dot{\theta} - \cos\theta\left[E_1(\cos\theta, -\dot{\theta}) + \frac{1}{k}E_6(\sin\theta, 0) + I_2\right] + \sin\theta\left[E_2(\sin\theta, \dot{\theta}) + \frac{1}{k}E_5(\cos\theta, 0) + I_1\right]. \tag{61}$$

Eqs. (60) and (61) are the ones presented in the section on static accuracy.

Minimization of the Partially-Developed Transfer Tree*

MITCHELL P. MARCUS†

Summary—**A transfer tree is a particular type of multiterminal network having a single input which may be connected to any one of a number of outputs.**

An n-relay transfer tree is partially developed if it has less than the 2^n possible output terminals. Rearrangement of a partially-developed tree can lead to a reduction in the total number of transfers required.

This paper presents a method of obtaining a required partially-developed transfer tree with the minimum number of transfers.

Introduction

A TRANSFER TREE[1,2] is a particular type of multiterminal relay network having a single input which may be connected to any one of a number of outputs. One and only one output is connected to the input at a given time, the selection being controlled by the combination of network relays operated. Each input-to-output path passes through one and only one contact on each relay in the network, and all outputs are disjunctive.

The number of possible relay combinations with n relays is 2^n; therefore, in an n-relay transfer tree there are 2^n possible outputs. A fully-developed tree has an output terminal for each of the 2^n possible relay combinations, and the total number of transfers in the tree is $2^n - 1$. A partially-developed tree has less than 2^n output terminals, and the total number of transfers in the tree may vary.

By the rearrangement of a fully-developed tree, the contact load on all relays except the first may be made more uniform; however, regardless of the arrangement, the total number of transfers in the tree remains $2^n - 1$. Rearrangement of a partially-developed tree, on the other hand, can lead to a reduction in the total number of transfers required.

The majority of transfer trees used in switching circuits are partially developed, and it is desirable that there be a method of minimizing them, *i.e.*, obtaining a required tree with the minimum number of transfers,

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[2] W. Keister, A. E. Ritchie, and S. H. Washburn, "The Design of Switching Circuits," D. Van Nostrand Co., Inc., New York, N. Y.; 1951.

and recognizing that the solution is a minimal one. All possible arrangements of a tree could, of course, be obtained, and the minimal one selected, but this process is long and laborious, prohibitively so in many cases. Table I gives some indication of the progressive complexity of a trial and error approach as n increases.

TABLE I

Number of relays in tree	Number of possible arrangements of fully-developed tree
2	$2^1 =$ 2
3	$3^1 \cdot 2^2 =$ 12
4	$4^1 \cdot 3^2 \cdot 2^4 =$ 576
5	$5^1 \cdot 4^2 \cdot 3^4 \cdot 2^8 =$ 1,658,880
6	$6^1 \cdot 5^2 \cdot 4^4 \cdot 3^8 \cdot 2^{16} =$ 16,511,297,126,400

The number of possible arrangements of an n-relay tree is represented by

$$[n^{2^0}][(n-1)^{2^1}][(n-2)^{2^2}][(n-3)^{2^3}] \cdots [2^{2^{n-2}}]$$

If P represents the number of possible arrangements of an n-relay tree, then the number of possible arrangements of an $(n+1)$-relay tree is $(n+1)P^2$.

This paper presents a method of minimizing partially-developed transfer trees.

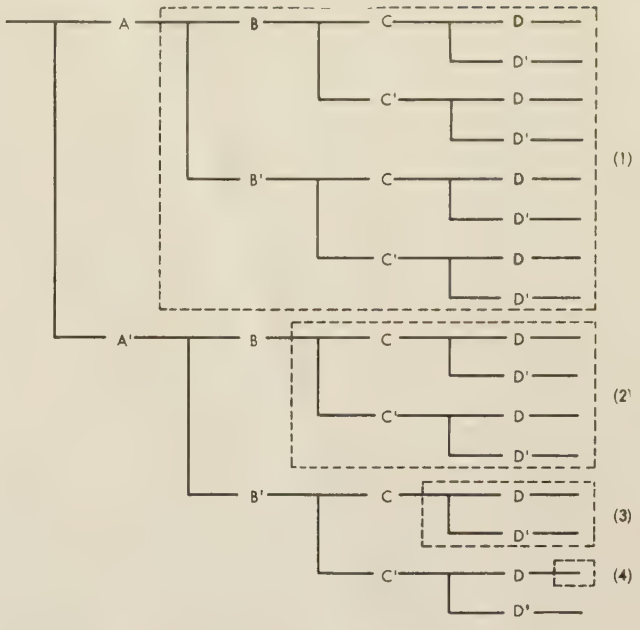
Basis for Method

In a fully-developed transfer tree, such as the one shown for reference in Fig. 1, a branch (minor tree) representing 2^x combinations contains 2^x-1 transfers. For example, in Fig. 1, the branch labeled (2) represents four combinations and contains three transfers; the branch labeled (4) represents one combination and contains no transfers.

A particular partially-developed tree can be obtained by starting with a fully-developed tree and removing the branches representing the groups of invalid output combinations. The removal of a branch representing a group of 2^x invalid combinations results in the elimination of 2^x-1 transfers. For instance, in Fig. 1, if the four combinations $A'BCD$, $A'BCD'$, $A'BC'D$ and $A'BC'D'$ were invalid, the branch labeled (2), representing this group of four combinations, could be removed, eliminating three transfers.

It follows that the total number of transfers eliminated equals the number of invalid combinations minus the number of groups into which these combinations are combined. The method of minimizing a partially-developed tree, therefore, consists of starting with a hypothetical fully-developed tree and eliminating the maximum number of transfers by arranging the order of the relays in the tree such that the invalid combinations can be combined into the minimum number of groups.

The key to the method, then, lies not in the analysis of the valid relay combinations, but rather in the analysis of the invalid combinations.



Branch (1) represents 8 combinations and contains 7 transfers.
Branch (2) represents 4 combinations and contains 3 transfers.
Branch (3) represents 2 combinations and contains 1 transfer.
Branch (4) represents 1 combination and contains 0 transfers.
Removal of a branch representing 2^x combinations results in the elimination of 2^x-1 transfers.

Fig. 1—Fully-developed transfer tree.

Method

In this paper, maps (charts)[3,4] are used as the means for combining the invalid combinations and obtaining the optimum order of the relays in the tree. There are notable differences, however, between the normal use of the maps and their use here; in this method 1) the invalid rather than the valid combinations are of prime consideration, 2) each combination is not considered as often as desired but is considered only once, and 3) the groups formed must be compatible with fundamental transfer tree configuration.

The use of the map to obtain any desired partially-developed n-relay tree (not necessarily a minimal one) will be described first.

An n-variable map is drawn, and an X is entered in each square representing a valid combination, as illustrated in Fig. 2 (next page). The map is then divided into two $(n-1)$-variable submaps, the divided variable becoming an adjunct to one submap, and the negative of the divided variable becoming an adjunct to the other submap. In each submap, the adjunct to that submap is written in the lower left-hand corner of each square representing a valid combination. (See Fig. 3.) (The particular order of subdivision used in the running example leads to a minimal tree; the basis for arriving at this optimum order will be apparent later, and the example will be reviewed from this standpoint.)

[3] E. W. Veitch, "A chart method for simplifying truth functions," *Proc. Association for Computing Machinery;* May, 1952.
[4] M. Karnaugh, "The Map Method for Synthesis of Combinational Logic Circuits," AIEE Tech. Paper 53-217; 1953.

Valid Combinations
A B C D
A B C D'
A B C'D
A B C'D'
A B'C D'
A'B'C D
A'B'C D'
A'B'C'D

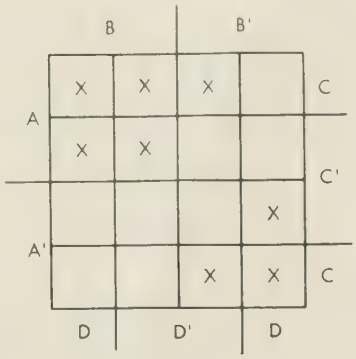


Fig. 2—Map related to partially-developed tree.

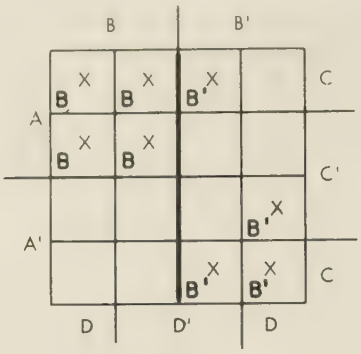


Fig. 3—First subdivision.

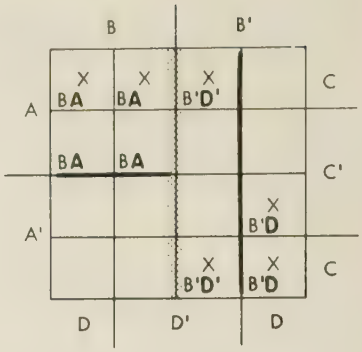


Fig. 4—Second and third subdivisions.

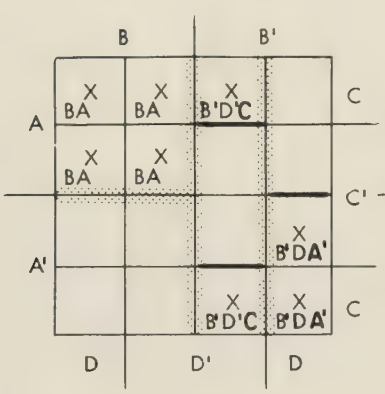


Fig. 5—Fourth and fifth subdivisions.

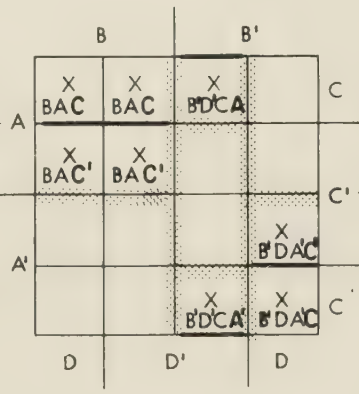


Fig. 6—Sixth and seventh subdivisions.

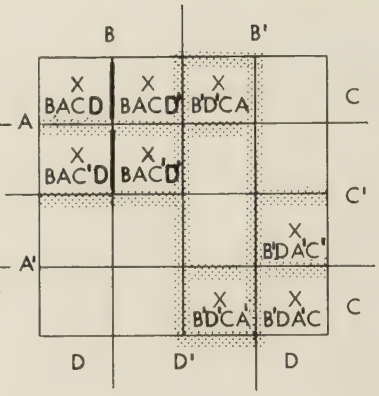


Fig. 7—Eighth subdivision.

Each $(n-1)$-variable submap containing a valid combination is subdivided into two $(n-2)$-variable submaps, the newly-formed adjunct in each case being written to the right of the previously-written adjunct. (See Fig. 4.) A submap containing only invalid combinations is not further subdivided. An invalid-combination submap containing 2^x squares represents the elimination of 2^x-1 transfers.

The subdivision process is continued until each valid square becomes a submap; all other submaps will contain only invalid squares. (See Figs. 5–7.) The designation of each valid combination will be completely written at the bottom of its representative square. The transfer tree can then be drawn with reference to these written designations, each input-to-output path from left to right corresponding to the equivalent order of the related written combination. (See Fig. 8.)

The order of subdivision determines the order of the relay contacts in the tree; the writing of the adjuncts in the valid squares is the means of recording the order of subdivision so that the transfer tree can be drawn by reference to the map; the subdivision process insures that the submaps formed will be compatible with transfer tree configuration.

Any order of subdivision will lead to a legitimate tree. However, to obtain a desired tree having the minimum number of transfers, the map must be subdivided such

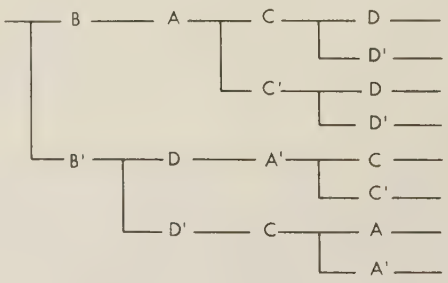
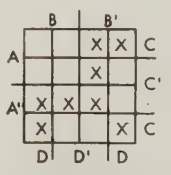


Fig. 8—Partially-developed transfer tree obtained from Fig. 7.

that the number of invalid-combination submaps is a minimum. The procedure is to combine the invalid combinations into the minimum number of groups that can be obtained by the subdivision process[5] (there may be

[5] In the following map, it is possible to combine the invalid combinations into three groups (AB, $A'CD'$, $B'C'D$); however, these three groups cannot be collectively obtained by the subdivision process (they are not compatible with transfer tree configuration). The minimum number of groups of invalid combinations that can be obtained by the subdivision process is four.



Map A

more than one way of doing this), and then subdivide the map to form the desired groups (there may be more than one way of doing this, also).

This was the procedure followed in the running example, as a review of the example will illustrate. Analysis of the map in Fig. 2 shows that the minimum possible number of groups of invalid combinations is three ($A'B$, $B'C'D'$ and $AB'D$), and that these groups can be obtained by the subdivision process. Furthermore, to form these three particular groups, the map must be subdivided as illustrated in Figs. 3-5. The tree obtained (Fig. 8) is, therefore, a minimal one.

The foregoing method may be modified; for instance, the subdivision process may be continued only until all invalid-combination submaps have been formed, as illustrated by Fig. 5; from the map at this stage, the tree can be partially constructed, and the rest completed by inspection. Fig. 9 shows the portion of the tree obtained from the map in Fig. 5. Branch removal has been completed and the rest of the tree can be drawn by inspection.

Following is a summary of the relationships involved:

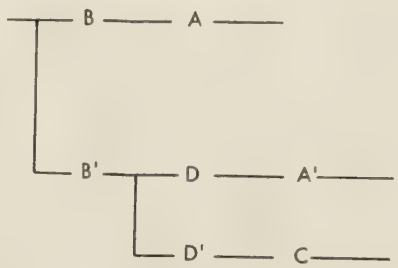


Fig. 9—Portion of tree obtained from Fig. 5.

n = number of relays in tree.
2^n = number of output combinations in fully-developed tree.
(2^n-1) = number of transfers in fully-developed tree.
m = number of invalid output combinations.
(2^n-m) = number of valid output combinations.
p = number of invalid-combination submaps.
$(m-p)$ = number of transfers eliminated from fully-developed tree.
$(2^n-1)-(m-p)=(2^n-m)+p-1$ = number of transfers in partially-developed tree.

A New Diode Function Generator*

T. MIURA†, H. AMEMIYA‡, AND T. NUMAKURA†

Summary—**With the diode function generators that are currently in use, generation of functions is made by combining straight lines. The main drawback of these function generators is that the slope of the line segment cannot be changed independently. With the new function generator described in this paper, functions are generated by connecting independent line segments. Accordingly, the slope of each segment is given independently and also quantitatively. It is possible to approximate any desired function without recourse to an oscilloscope for inspection. These advantages are realized by using ganged potentiometers differentially. The operating principle and a practical generator experimentally built are described.**

Introduction

THE DIODE function generators are very useful as components of electronic analog computers. However, those generators currently available are not convenient to use because of their inherent disadvantage that the slopes of line segments constituting a function cannot be changed independently. This is because a function is generated by superposing linearly-increasing functions starting at certain input voltages, such as shown in Fig. 2(a). With the new function generator, a function is produced by superposing constituent functions, which increase linearly for certain input voltage ranges and which level off beyond, [Fig. 1(a)]. Therefore, the slope of each line segment of the resultant function is produced in the same manner but independently of others. Any desired function can be generated very easily and yet quantitatively.

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Operating Principle of the New Diode Function Generator

Figs. 1 and 2 show how a function is generated by the new and by the conventional diode function generators. The function to be generated is shown at the top in both figures and is expressed by

$$\begin{aligned}[e_0]_{E_n<e_i<E_{n+1}} &= (E_2-E_1)\tan\theta_1 \\ &\quad + (E_3-E_2)\tan\theta_2 \\ &\quad \cdots\cdots\cdots \\ &\quad + (E_n-E_{n-1})\tan\theta_{n-1} \\ &\quad + (e_i-E_n)\tan\theta_n \\ &= \sum_{j=1}^{n-1}(E_{j+1}-E_j)\tan\theta_j + (e_i-E_n)\tan\theta_n \\ &= \sum_{j=1}^{n} e_{0j}, \end{aligned} \tag{1}$$

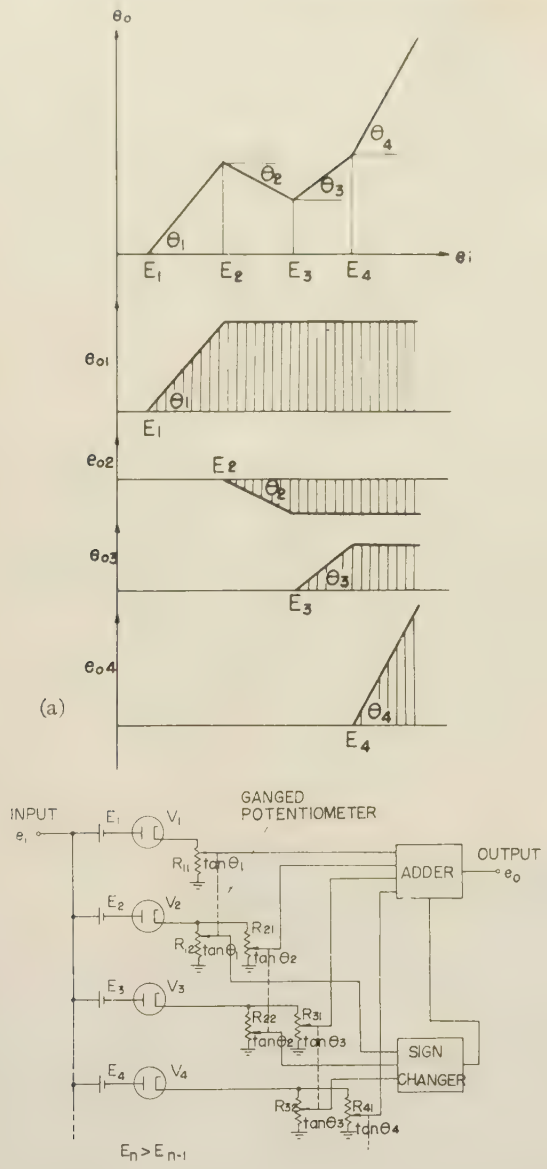


Fig. 1—Operating principle and basic circuit of the new diode function generator.

where

$$e_{0j} = (E_{j+1} - E_j) \tan \theta_j,$$

and

$$e_{0n} = (e_i - E_n) \tan \theta_n.$$

Eq. (1) may be rearranged as

$$\begin{aligned}[e_0]_{E_n<e_i<E_{n+1}} &= (e_i - E_1) \tan \theta_1 \\ &\quad + (e_i - E_2)(\tan \theta_2 - \tan \theta_1) \\ &\quad + (e_i - E_3)(\tan \theta_3 - \tan \theta_2) \\ &\quad \cdots\cdots\cdots\cdots \\ &\quad + (e_i - E_n)(\tan \theta_n - \tan \theta_{n-1}) \\ &= \sum_{j=1}^{n} (e_i - E_j)(\tan \theta_j - \tan \theta_{j-1}) \\ &= \sum_{j=1}^{n} (e_i - E_j) \tan \Theta_j \\ &= \sum_{j=1}^{n} e_{0j}' \end{aligned} \tag{2}$$

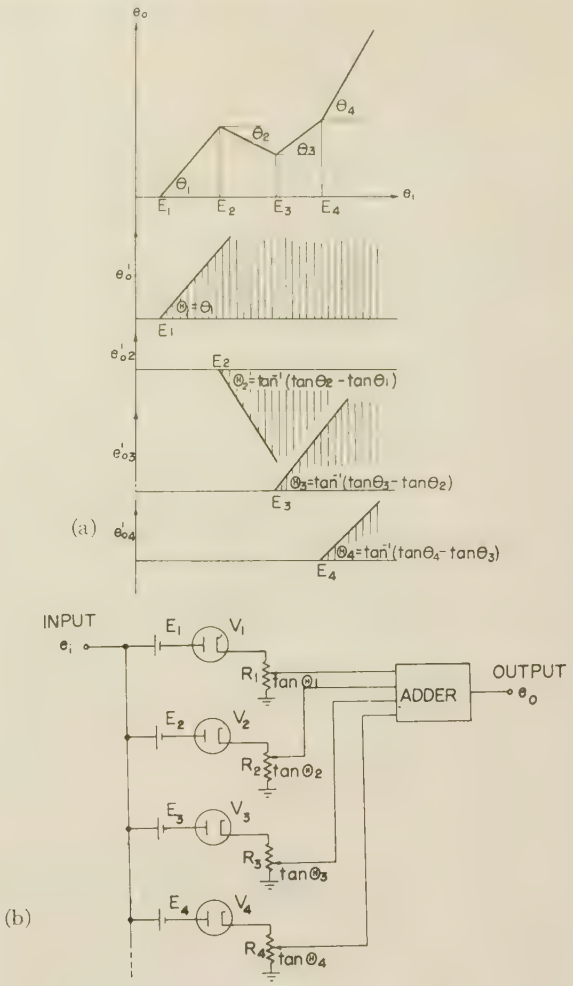


Fig. 2—Operating principle and basic circuit of the conventional diode function generator.

where

$$e_{0j}' = (e_i - E_j) \tan \Theta_j, \quad \tan \Theta_j = \tan \theta_j - \tan \theta_{j-1},$$

and

$$\tan \theta_0 = 0.$$

With the conventional function generator, the desired function is obtained by realizing the relation expressed by (2). The terms of (2) are shown separately in Fig. 2(a). By adding these voltages, the desired function is obtained.

Fig. 2(b) is a basic circuit to achieve this. E's are individual bias voltages, V's are diodes, and R's are potentiometers. The diodes conduct only if the input voltage e_i is higher than the respective bias voltages, thus giving straight lines starting at the bias voltages. The potentiometers are used to give slopes to these lines.[1] Now it is clear that the slopes of line segments of the resulted function are closely interrelated. For instance, if tan Θ_2 is changed to vary the slope tan θ_2, all the slopes of the following segments, such as tan θ_3, tan θ_4, etc., change simultaneously. This is a disadvantage of

[1] Although not shown in the figure to avoid confusion, a sign changer is necessary between the potentiometer and the adder when the slope tan Θ_j is negative. In the example given here, a sign changer must be used after R_2, because tan Θ_2 is negative.

the function generator of this type, because this makes it troublesome to adjust the settings of potentiometers to obtain precisely the desired function.

With the new diode function generator, the function is generated by realizing (1) literally term by term. As shown in Fig. 1(a), each constituting voltage e_{0j} has a slope prescribed by the function for $E_j < e_i < E_{j+1}$ and then levels off. The function is obtained by adding these voltages. Fig. 1(b) shows how this is done. Here, E's are bias voltages and V's are diodes as in Fig. 2(b), and R's are ganged potentiometers. The bias voltage E_1, the diode V_1, and the potentiometer R_{11} give a line with a slope of tan θ_1 starting at $e_i = E_1$. Similarly, E_2, V_2, and R_{12} give a line with the same slope, because R_{11} and R_{12} are ganged, but starting at $e_i = E_2$. The output from R_{11} is fed directly to the adder, whereas the output from R_{12} is fed first to the sign changer and then to the adder. Therefore, the output of the adder contributed by these two circuits has the slope of tan θ_1 for $E_1 < e_1 < E_2$ and is constant for $E_2 \leqq e_i$ as shown by e_{01} of Fig. 1(a). Voltages e_{02}, e_{03}, etc. are obtained in exactly the same way. Since the output voltage e_0 is the sum of these voltages, the slopes of the line segments are given independently by individual potentiometers, and there is no relation either explicit or implicit, between these slopes.

The practical diode function generator built on the principle described in the preceding paragraphs has construction somewhat different from Fig. 1(b). The basic circuit is shown in Fig. 3, where potentiometers are not grounded so that the slopes of the line segments can have either positive or negative values according to their settings. In Fig. 3, the output voltage is given by

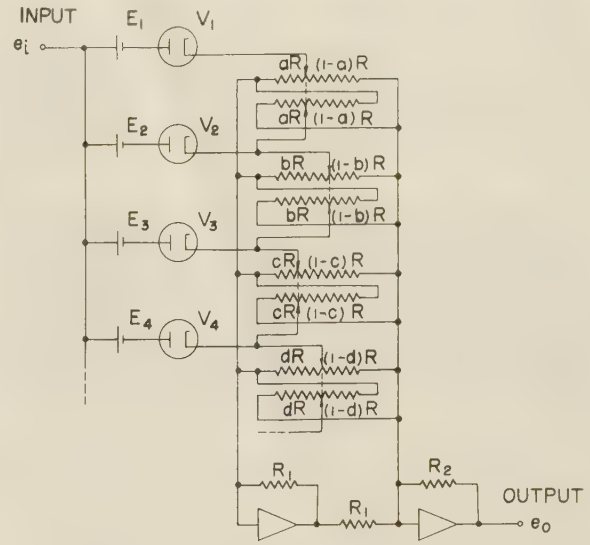


Fig. 3—Basic circuit of the new diode function generator experimentally built.

The equation shows that the slopes, which are given by

$$\left(\frac{1}{a} - \frac{1}{1-a}\right)\frac{R_2}{R}, \qquad \left(\frac{1}{b} - \frac{1}{1-b}\right)\frac{R_2}{R}, \text{ etc.,}$$

may take either positive or negative values and are given independently by respective ganged potentiometers.

Practical Diode Function Generator

Fig. 4 (next page) is the circuit diagram of the new diode function generator that gives eight independent

$$\begin{aligned}
[e_0]_{E_n<e_i<E_{n+1}} &= (e_i - E_1)\left\{\frac{R_1}{aR}\frac{R_2}{R_1} - \frac{R_2}{(1-a)R}\right\} \\
&\quad + (e_i - E_2)\left\{\frac{R_1}{(1-a)R}\frac{R_2}{R_1} - \frac{R_2}{aR} + \frac{R_1}{bR}\frac{R_2}{R_1} - \frac{R_2}{(1-b)R}\right\} \\
&\quad + (e_i - E_3)\left\{\frac{R_1}{(1-b)R}\frac{R_2}{R_1} - \frac{R_2}{bR} + \frac{R_1}{cR}\frac{R_2}{R_1} - \frac{R_2}{(1-c)R}\right\} \\
&\quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&\quad + (e_i - E_n)\left\{\frac{R_1}{(1-m)R}\frac{R_2}{R_1} - \frac{R_2}{mR} + \frac{R_1}{nR}\frac{R_2}{R_1} - \frac{R_2}{(1-n)R}\right\} \\
&= (E_2 - E_1)\left(\frac{1}{a} - \frac{1}{1-a}\right)\frac{R_2}{R} \\
&\quad + (E_3 - E_2)\left(\frac{1}{b} - \frac{1}{1-b}\right)\frac{R_2}{R} \\
&\quad \cdots\cdots\cdots\cdots \\
&\quad + (e_i - E_n)\left(\frac{1}{n} - \frac{1}{1-n}\right)\frac{R_2}{R}. \qquad (3)
\end{aligned}$$

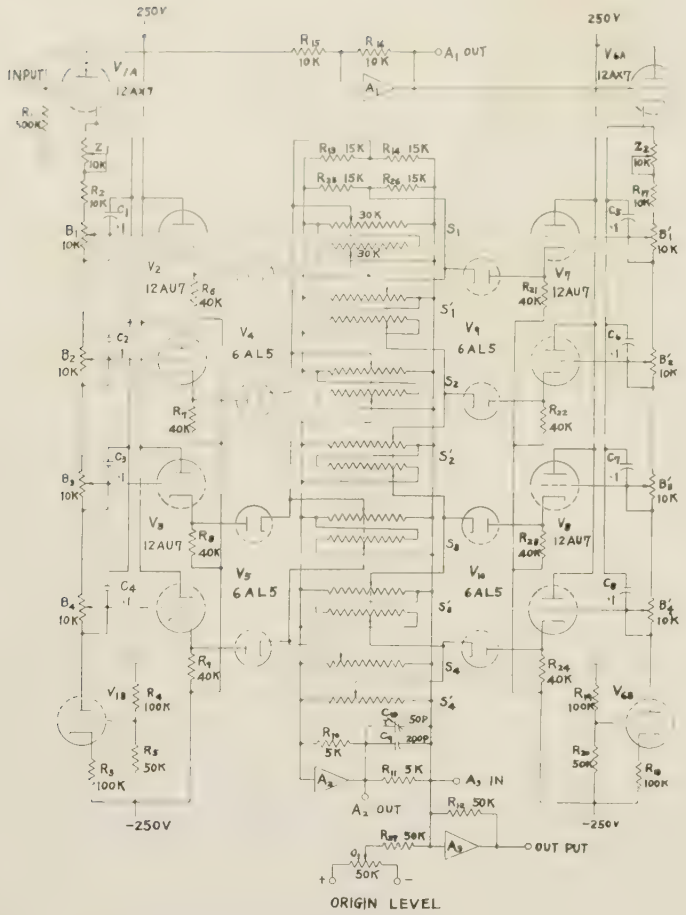


Fig. 4—Circuit diagram of the new diode function generator.

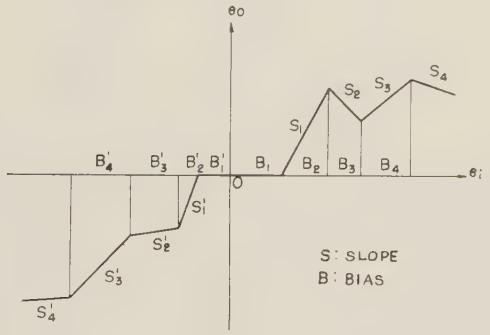


Fig. 5—Slope and bias potentiometers are used to control the segments shown.

line segments, namely, four on the plus side and four on the minus side, as shown in Fig. 5.

The constant current circuit consisting of V_1 and of its associated potentiometers, B_1, B_2, B_3, and B_4, and the cathode followers, V_2 and V_3, replace the individual sources of bias voltage, E_1, E_2, etc., in Fig. 3.[2] A perfect constant current characteristic insures the same gain from the input to the grids of all the cathode followers, V_2 and V_3, which is very important to obtain the aforementioned independency of slopes. Capacitors, C_1, C_2, C_3, and C_4, are used to maintain the same gain up to

[2] The circuit was designed after Function Fitter, manufactured by G. A. Philbrick Researches, Inc., Boston, Mass.

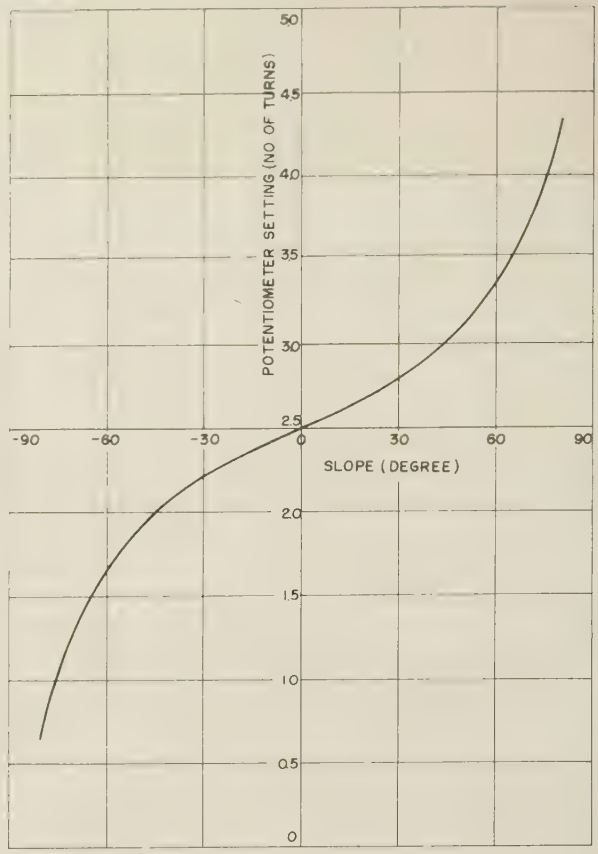


Fig. 6—Calibration curve of slope vs potentiometer dial setting.

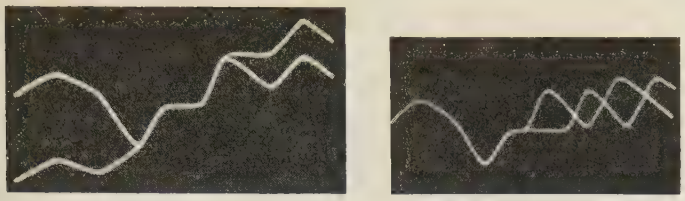
high frequencies where stray capacities tend to decrease it. Thirty kilo-ohm, 5-turn helical potentiometers of good linearity are used for slope potentiometers. The internal resistance of the diode circuit, that is, the resistances of the cathode follower and the diode rectifier in series, must be low to obtain the independency of slopes.[3] Practically, however, this requirement is somewhat alleviated by equalizing the diode loading by attaching R_{13} and R_{14} to the first diode.

Functions for negative values of e_i are generated in exactly the same manner as for positive values, with the only difference being that a sign changer, A_1, is used at the input. Potentiometers, Z_1 and Z_2, are zero (origin) adjustments of the bias potentiometers, and C_9 and C_{10} are to compensate for the phase lag of the operational amplifier A_2. The output dc level of A_2 is adjusted with the input of A_3 grounded as otherwise the output dc voltage of A_3 feeds back to the input of A_2 making the level adjustment impossible.

Fig. 6 shows the relation between slope and potentiometer setting. The curve was experimentally obtained and applies to all the slope potentiometers with very little error. It is possible to set desired slopes by referring only to this curve, without recourse to an oscilloscope for inspection. Bias voltage is 8.6 volts when the bias potentiometer is placed at the full-counterclockwise position.

Fig. 7 shows a function generated by the new func-

[3] Appendix I.



(a) (b)

Fig. 7—Independency of slope and independency of bias are shown in 7(a) and 7(b), respectively.

tion generator. Fig. 7(a) illustrates visually the independency of slopes. The picture was taken by double exposure changing the settings of potentiometers, S_2 and S_2'. It should be noted that the other slopes are not changed at all. Fig. 7(b) shows the independency of bias adjustment. Bias potentiometer B_1 was turned with a mere shift of a part of the generated function. In Fig. 8, the absolute value characteristic and square characteristic are approximated. Fig. 8(a) and 8(c) are by 400 cps input; 8(b) and 8(d) by 1 kc input. It is supposed that the phase shift at 1 kc is about one degree or two.

Conclusion

A new diode function generator described in this paper is believed to be a very powerful addition to analog computers because of its extreme versatility and also of its easy but quantitative generation of any desired function. The principle on which this new function generator is based may also be applied to obtain a limiter with ideal characteristic.[4]

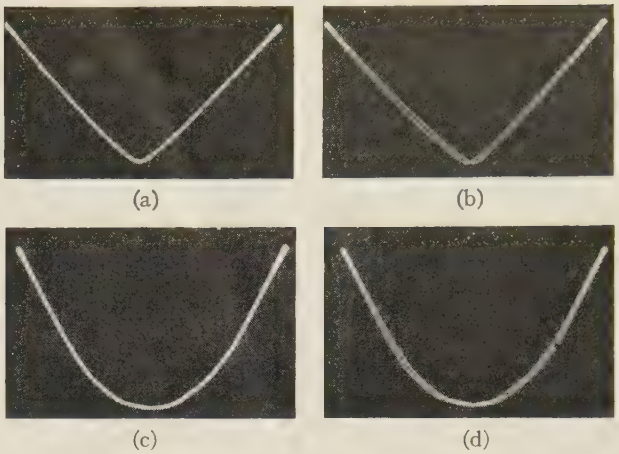
Appendix I

If the internal resistances of the diode circuits are taken into consideration, (3) becomes

$$
\begin{aligned}
[e_0]_{E_n<e_i<E_{n+1}} &= (e_i - E_1)\frac{R_A}{R_{i1}+R_A}\left\{\frac{R_1}{aR}\frac{R_2}{R} - \frac{R_2}{(1-a)R}\right\} \\
&\quad + (e_i - E_2)\frac{R_B}{R_{i2}+R_B}\left\{\frac{R_1}{(1-a)R}\frac{R_2}{R_1} - \frac{R_2}{aR} + \frac{R_1}{bR}\frac{R_2}{R_1} - \frac{R_2}{(1-b)R}\right\} \\
&\quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&\quad + (e_i - E_n)\frac{R_N}{R_{in}+R_N}\left\{\frac{R_1}{(1-m)R}\frac{R_2}{R_1} - \frac{R_2}{mR} + \frac{R_1}{nR}\frac{R_2}{R_1} - \frac{R_2}{(1-n)R}\right\} \\
&= \left\{e_i\left(\frac{R_A}{R_{i1}+R_A} - \frac{R_B}{R_{i2}+R_B}\right) + E_2\frac{R_B}{R_{i2}+R_B} - E_1\frac{R_A}{R_{i1}+R_A}\right\}\left(\frac{1}{a} - \frac{1}{1-a}\right)\frac{R_2}{R} \\
&\quad + \left\{e_i\left(\frac{R_B}{R_{i2}+R_B} - \frac{R_C}{R_{i3}+R_C}\right) + E_3\frac{R_C}{R_{i3}+R_C} - E_2\frac{R_B}{R_{i2}-R_B}\right\}\left(\frac{1}{b} - \frac{1}{1-b}\right)\frac{R_2}{R} \\
&\quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&\quad + \left\{(e_i - E_n)\frac{R_N}{R_{in}+R_N}\right\}\left(\frac{1}{n} - \frac{1}{1-n}\right)\frac{R_2}{R},
\end{aligned}
$$

where R_i's are the internal resistances and

[4] Appendix II.



(a) (b) (c) (d)

Fig. 8—Absolute value characteristic and square characteristic are approximated. Figs. 8(a) and 8(c) are by 400 cps input, and 8(b) and 8(d) by 1 kc input.

$$R_A = a(1-a)R,$$

$$R_B = \frac{a(1-a)b(1-b)}{a(1-a)+b(1-b)}R,$$

. . . . . .

and

$$R_N = \frac{m(1-m)n(1-n)}{m(1-m)+n(1-n)}R.$$

Independency of slopes of line segments is attained if the condition

$$\frac{R_A}{R_{i1}+R_A} = \frac{R_B}{R_{i2}+R_B} = \cdots = \frac{R_N}{R_{in}+R_N}$$

is satisfied. Ideally, $R_{i1}=R_{i2}=\cdots=R_{in}=0$ is the only solution. If the resistance of potentiometer is made high, it is possible to realize $R_A \gg R_{i1}$, $R_B \gg R_{i2}$, $\cdots$, $R_N \gg R_{in}$ to satisfy the above condition. This is not recommended, however, for a function generator of high-speed analog computers for which good high-frequency response is essential.

Appendix II

Ordinary limiter circuits give a final slope of

$$\left[\frac{de_0}{de_i}\right]_{E<e_i} = \frac{R_i}{R + R_i} > 0$$

as shown in Fig. 9. To idealize the characteristic and make the final slope zero, R must be made very large in comparison with R_i, which limits the useful frequency range.

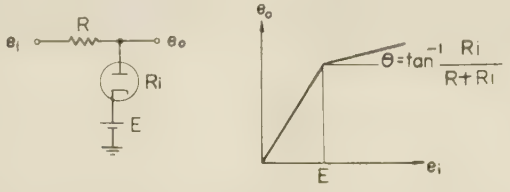


Fig. 9—Ordinary limiter circuit and its characteristic.

If a circuit is arranged so that the output from a dead zone circuit is subtracted from the input as shown in Fig. 10, a limiter with ideal characteristic, or even with a negative final slope, is obtained. The frequency response of this ideal limiter can be made sufficiently wide to cover the necessary frequency range of repetitive

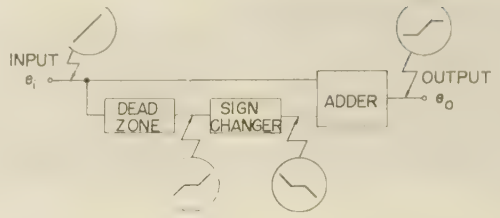


Fig. 10—Block diagram of the new limiter with ideal characteristic.

analog computers. It is recommended that a switch be provided so that the equipment may be used both as a limiter and as a dead zone simulator.

Acknowledgment

The authors wish to express their sincere gratitude to Professor Tamiya Nomura of the Institute of Industrial Science, the University of Tokyo, for his kindness in supplying freely the pertinent experimental data and also to Dr. Bunya Tadano and Zen'emon Abe of Hitachi Central Research Laboratory, whose advice was invaluable in performing the study. Last but not least, the authors wish to thank Takeshi Kinugawa of Hitachi Central Research Laboratory and Takeshi Hasegawa of Showa Denshi, Ltd., whose cooperation was particularly helpful.

An Electronic Analog Multiplier*

DAVID C. KALBFELL†

Summary—**This multiplier uses the variable pulse area principle, but employs phase sensitive circuitry to operate naturally in all four quadrants without bias voltages. The output is zero if either input is zero. The X and Y channels are separately linearized with independent feedback loops. The circuitry is simple and lends itself to either transistors or vacuum tubes.**[1]

A GOOD electronic multiplier should have several characteristics: 1) It should operate correctly in all four quadrants; that is, X and Y may be either positive or negative. 2) Bias voltages should not be added to the variables, to permit four-quadrant operation, since these bias voltages may drift and cause errors. 3) The rise time for transient changes should be no greater than 10 milliseconds. 4) The circuit should be inherently free of drift and be fairly linear without feedback. 5) Negative feedback should be incorporated in the X and Y channels of the multiplier separately, so that each is independently linearized and compensated for drift. 6) The whole circuit should be simple and require a small number of vacuum tubes.

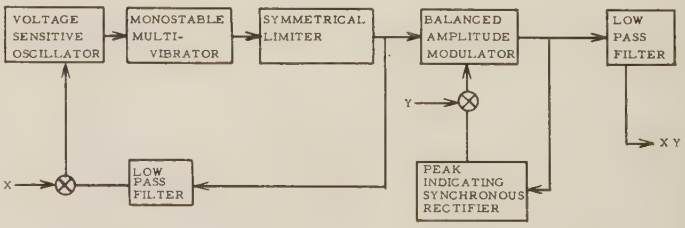


Fig. 1.

Fig. 1 illustrates the basic operating principles of this new electronic multiplier. One variable, X, controls the width of pulses; while the other variable, Y, controls the height of the pulses. Phase sensitive circuitry is

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[1] Patent pending on this device.

employed to keep track of the signs of X and Y, so that bias voltages are unnecessary. The X voltage controls the frequency of a voltage-sensitive oscillator, such as a multivibrator. This might typically operate at a frequency of 100 kc. The output of this voltage-sensitive oscillator fires a monostable multivibrator. The duration of the metastable state of this multivibrator is determined by an inert delay line. If the voltage-sensitive oscillator puts out a frequency of 100 kc when $X=0$, then the delay line should be 5 microseconds long.

This unsymmetrical waveform is now passed through a blocking capacitor and is clamped symmetrically with respect to ground. This symmetrically clamped wave will now contain a dc component which is directly proportional to the original X modulating voltage except for such nonlinearities as might have been introduced by the system up to this point. The dc and low-frequency components of this unsymmetrical wave are now fed back to the input as negative feedback. For ordinary computer applications, X would have a full-scale value of 100 volts, although 10 volts would probably be sufficient to produce the desired degree of modulation of the oscillator. If the feedback voltage is 90 volts when the input voltage is 100 volts, this will act like 20 db of negative feedback and will compensate drifts and nonlinearities. For a superior system, the X voltage might have been fed to the voltage-sensitive oscillator through a preamplifier. If the feedback voltage is mixed with X at the input of the preamplifier, then a larger feedback factor might be employed and the frequency of the voltage-sensitive oscillator could be deviated through a wider range, thus making the latter portion of the equipment function more accurately.

The first section of this system functions as a unit including its own stabilization, and merely feeds a clamped unsymmetrical waveform to the amplitude modulator. This modulator converts the clamped amplitude into a variable amplitude which is proportional to Y. This might be accomplished in a ring modulator or by several alternative means. The output of this modulator is used in two ways. First, a feedback signal must be derived from it to buck against the Y signal to give negative feedback around the amplitude modulator section of the system. In order to give the correct sign and to be independent of X, the amplitude of the modulator output is sensed and this is passed through a switching system which insures that the correct sign of feedback voltage is always bucked against Y, regardless of the original sign of Y. One method of accomplishing this synchronous rectification will be described later. The second use to which the output of the amplitude modulator is put is to give the product of X and Y after passing through a low-pass filter. The output of this low-pass filter may be either positive or negative, depending upon the original signs of X and Y. If either X or Y is 0, the output will be 0.

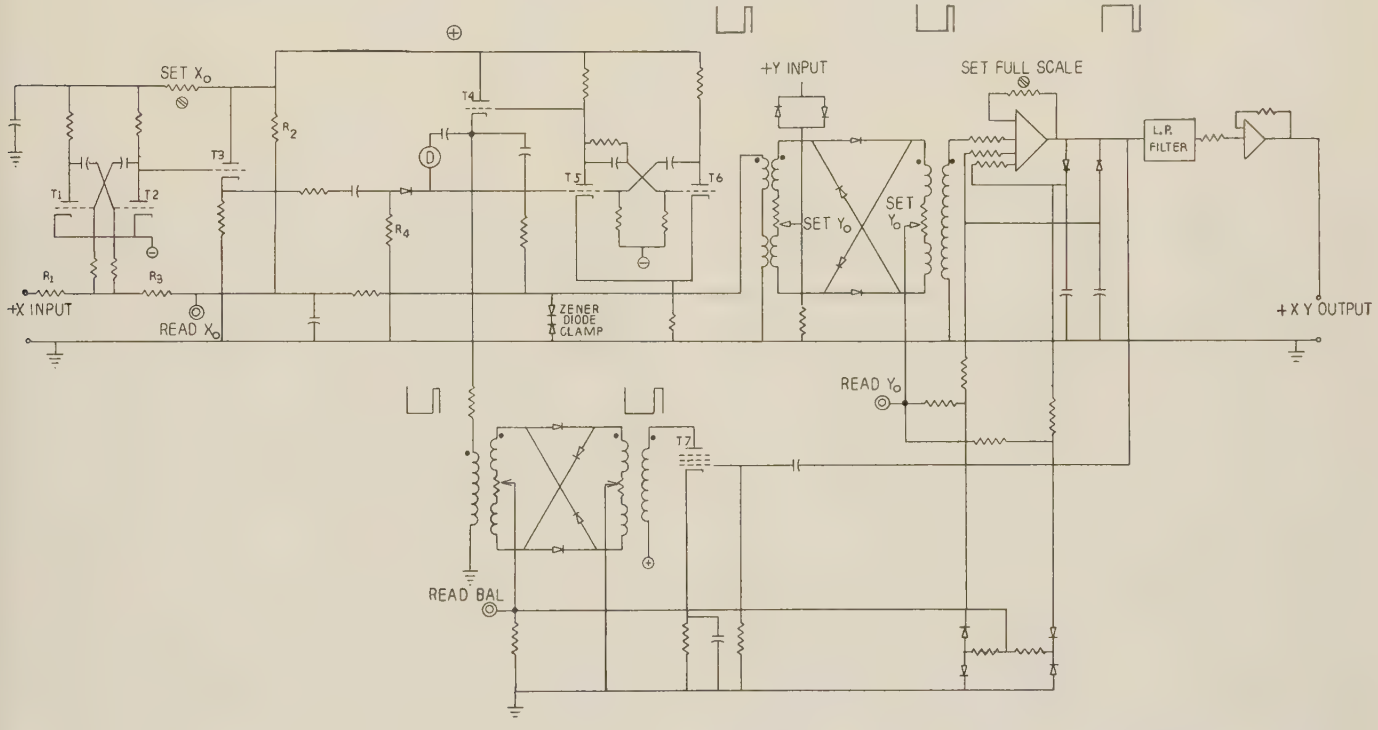

Fig. 2.

Fig. 2 is a more detailed circuit diagram showing one method for making an electronic multiplier of the type

which has been described. The X input is applied to the bottoms of the grid leaks of a multivibrator operating at a frequency of 100 kc. In practice, it might be desirable to make a somewhat more sophisticated form of multivibrator in order to give better stability and sharper cornered waves. This is an engineering detail which does not concern the present design, however. The multivibrator output is buffered through a cathode follower and triggers the monostable multivibrator. T5 is normally cut off, since its grid leak is returned to a negative bias voltage. A positive pulse from T3 causes T5 to fire, which cuts off T6. When T5 fires, its plate voltage drops and a negative pulse is fed through T4 to a delay line. The delay line, D, should be 5 microseconds long for the example being discussed. When the negative pulse comes out of the delay line, it cuts off T5, thus resetting the monostable multivibrator to its initial state. When the negative pulse comes out of the delay line, its energy is partly drained to ground through the diode and resistor R4. This need not cause any trouble, however, since R4 may be picked to be the optimum terminating resistor for the delay line.

The waveform sketches which are indicated throughout this figure are drawn on the assumption that X is positive and Y is positive.

The voltage at the cathode of T4 is fed through a series resistor and capacitor to a symmetrical clamp. This clamped voltage is fed through a low-pass filter, cutting off in the vicinity of 1 kc, back to the input terminal. Since the cathodes of T1 and T2 are tied to a negative potential, their grids would be negative and current would flow through their grid leaks from an input point at ground potential. R2 is inserted to provide current from a positive supply to just equalize the normal grid current of T1 and T2, so that the signal input point is normally at ground potential. If X is positive, it causes current to flow into these grid leaks. The feedback signal, however, is then negative and causes a negative current to flow into the grid leaks, largely cancelling the X input current. This system may be adjusted for drift by setting the X input point at ground and adjusting the variable resistor labelled "Set X_0" to make the potential at jack "Read X_0" come to ground potential. This part of the system is then adjustable and tends to be self-compensating.

The voltage from the cathode of T4 is now fed to the primary of a modulating transformer. For best stability, this voltage may well be taken from the point at which it is symmetrically clamped with respect to ground, in order to avoid amplitude variations due to tube aging. The Y input signal is applied to one side of this balanced ring modulator, and the Y feedback voltage is applied to the other side. The ring modulator is balanced by potentiometers at the center of each winding. This makes it possible to compensate for differences in the diodes. The polarity of winding of all transformers is indicated by dots at one end of each winding, and the waveforms are also indicated on the assumption that both X and Y are positive. The secondary voltage at the output of this ring modulator will have the same general type of wave shape as the input, although it would be inverted if Y were negative. In any case, its dc component has been lost in passing through the transformer, and so it must again be clamped symmetrically with respect to ground. Since the amplitude now contains part of our intelligence, however, we can no longer use a simple clamp for this purpose. Instead, peak indicating rectifiers are used to develop positive and negative voltages corresponding to the positive and negative amplitudes of the wave after passing through an operational amplifier. By feeding these two peak voltages into the input of the amplifier, the output is made symmetrical with respect to ground. This takes care of the clamping requirement.

The next portion of the circuit provides negative feedback voltage to correct for any nonlinearity or drift in the ring modulator and the operational amplifier. The pulses on the output of the operational amplifier are amplified further, so that they may be used even though their amplitude be less than one tenth (0.1) volt. T7 performs this amplification, and its plate current flows through the primary of another modulator transformer. If desired, these transformers could be shunt fed instead of carrying dc current. The other transformer on this modulator is fed from the cathode of T4 and provides a dc return path for the current of this tube. This modulator is balanced so that when the output of the operational amplifier is shorted to ground, 0 voltage is produced at the jack labelled "Read Bal." In order to provide appropriate feedback voltage which depends upon Y and not upon X, we must extract information which depends only upon the amplitude of the output of the operational amplifier, while being independent of its waveform. Since this output has already been clamped symmetrically with respect to ground, either peak indicating rectifier might be used for this purpose, but it is also essential that the correct sign be selected. This balanced modulator and the diode gate system which is fed by the modulator act as a synchronous switch to permit signal of only the correct sign to be applied to the Y feedback point of the Y amplitude modulator.

The operation of this synchronous switch will now be described. If the phases of all voltages are as indicated for X and Y, both being positive, then the balanced modulator of this synchronous switch system will put out a positive voltage. In this case, the left-hand pair of diodes of the synchronous switch will be clamped to ground, and the negative rectified voltage of the operational amplifier output will be shorted to ground and will make no contribution to the feedback signal. A positive signal from the modulator portion of this synchronous switch system would block off the right-hand pair of diodes so that they conduct no current, and hence the positive rectified voltage from the output of the operational amplifier will be applied to the Y feed-

back point. The proper sign of voltage will always be available. This system has the advantage that the magnitude of the feedback voltage is not dependent upon the nonlinearities of the switching system, but this amplitude will simply be proportional to the voltage on the peak indicating rectifiers. The rest of this feedback system merely acts as an on-off switch of the shunting type.

The final output of the multiplier consists of the average value of the output of the operational amplifier after passing through a low-pass filter. It may be adjusted to give 100 volts out when X and Y are each 100 volts, by adjusting the feedback resistor of the operational amplifier.

From this analysis, it is now apparent that this electronic multiplier system meets all of the requirements which were set forth in the first paragraph. If this ring modulator should get out of balance, it could only lead to an error for very small values of Y. Even with negative feedback, there will be some nonlinearity of the Y modulator at small amplitudes, and this is corrected by inserting some crystal diodes in series with the Y input, to compensate this error. The X and Y systems are separately stabilized with negative feedback, and provision is made for setting their 0 values. The system automatically operates in all four quadrants without the use of any bias voltages.

An Algorithm for Determining Minimal Representations of a Logic Function*

BERNARD HARRIS†

Summary—**For each logic function, or Boolean algebraic expression, there corresponds an appropriate computer circuit. However, the minimization of the appearances of the Boolean variables does not necessarily lead to the most economical circuit. A general approach to the problem therefore requires the development of techniques for the simple and rapid generation of a variety of near-minimal forms.**

This paper describes such a method for constructing the minimal representations of a logic function given as a truthtable or in one of its canonical forms. The minimal representations achieved are either sums of products, or products of sums, such that no term contains superfluous variables and such that no term is superfluous. The utility of the method lies in the conciseness of notation, which permits the handling of a large number of variables and simplifies the process for machine computation.

Introduction

FOR EACH logical truth function, or Boolean algebraic expression, there corresponds an appropriate switching circuit. However, the minimization of the appearances of the Boolean variables does not necessarily lead to the most economical circuit. A general approach to the problem therefore requires the development of techniques for the simple and rapid generation of a variety of near-minimal forms.

The direct application of Boolean algebra [1] is not completely satisfactory, since it involves the nonsystematic trial of a very large number of alternate procedures. A minimization chart, such as developed at the Harvard Computation Laboratory [2], represents an improvement, but the large number of entries renders the system cumbersome. The map method of Karnaugh [3] represents a further improvement because it permits the over-all system to be visualized. Unfortunately, however, these methods and their variations become difficult to apply when the number of independent variables greatly exceeds five.

The technique of assigning a decimal number to each minimal polynomial of the truthtable considerably improves the facility with which a large number of variables may be handled. The method introduced by Mueller [4] requires performing arithmetic operations with each decimal representation and checking whether the numbers so derived are present in the given list of decimal vertex numbers. By these comparisons, the decimal numbers are appropriately grouped into forms which permit expression by the fewest possible terms. The main disadvantage of this method lies in the necessity for the separate bookkeeping of indexes to determine the form of the solution.

The method described here is an extension of Mueller's idea, the terms of the canonical form being interpreted as though they were ternary numbers rather than binary. After these ternary numbers have been written as their decimal equivalents, the resulting numbers are manipulated without the necessity of having to refer to the truthtable again. The use of ternary notation permits not only the original entries of the truthtable to be assigned corresponding numbers, but the various groups as well. The solution then consists of a set of ternary numbers which directly corresponds to the appropriate groups.

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Theoretical Discussion

There exists a one-to-one correspondence between any possible terms of the canonical form of an n-independent-variable logic function and the vertices of an n-dimensional cube. The terms of the canonical form therefore correspond to a unique subset of the vertices of the n-dimensional cube. Let any face of this cube, all of the vertices of which are present in the truth function, represent a cell. The logic function may then in turn be represented by any set of cells which contains all of the required vertices at least once.

An irredundant covering of the truth function is a set of cells such that each vertex is included in at least one cell, and such that no cell is contained in a larger cell or in the covering of the other cells. This permits the truth function to be expressed as a sum of products such that no product is superfluous or contains a superfluous variable. By covering the complement of the logic function in a similar fashion the truth function may be expressed as a product of sums such that no sum is superfluous or contains a superfluous variable. In general, several such coverings exist, and the emphasis is on determining those combinations having the smallest possible number of cells.

Description of each vertex may be given by the appropriate binary number. Description of a cell, however, requires another symbol to indicate which variables are not required to describe the cell. This requirement may be met by using a ternary radix.

A simple coding scheme between the conventional binary notation and this ternary notation is to let the ternary zero and one correspond to the binary zero and one. The ternary two then corresponds to a condition in which both the binary zero and the binary one are included. Vertices are thus represented by all possible combinations of the ternary zeros and ones, while an r-dimensional cell is characterized by a ternary number containing the digit two in exactly r positions. Variations in the coding scheme are possible, but this choice permits the vertices to be designated by the smaller numbers and the higher order cells by the generally higher numbers.

As an example consider four vertices which may be combined into a second order cell.

$$\left.\begin{matrix}101000\\101001\\101100\\101101\end{matrix}\right\} 101202.$$

Considering these numbers to be in ternary notation and writing the equivalent decimal numbers gives

$$270 + 271 + 279 + 280 = 290.$$

The rule for this "addition" is that the "sum" of the numbers equals twice the largest minus the smallest. It is important to note that this rule is only a procedure for determining the proper number representing the $(r+1)$ cell *after* it has been determined that the proper vertices are being combined. The remaining problem lies in determining if the proper vertices are present.

Consider two vertices, numerically symbolized by conventional one and zeros, to be separated by a distance defined as the number of binary places by which they differ. The binary representation of these vertices may further be considered to be actual numbers written with some radix P. Then the necessary condition that these vertices be exactly a distance K apart in n-dimensional space is that the numerical difference of the corresponding vertex numbers be a number expressible in the form

$$\sum_{i=1}^{K} \alpha_i P^{k_i} \tag{1}$$

where $k_i \neq k_j$ is the degree of the positions where the numbers differ and α_i is either plus or minus one.

To show that this difference is a sufficient indication of the distance between vertices, consider any two vertices which are separated by a distance $H \neq K$. The numerical difference of the corresponding vertex numbers must then be of the form

$$\sum_{j=1}^{H} \beta_j P^{h_j} \tag{2}$$

and it is necessary to show that

$$\sum_{i=1}^{K} \alpha_i P^{k_i} \neq \sum_{j=1}^{H} \beta_j P^{h_j}. \tag{3}$$

Assume that an equality is possible and transfer those terms for which $\alpha_i = -1$ to the right and those terms for which $\beta_j = -1$ to the left. If an equality is possible, then

$$\sum_{i,\alpha_i=1} P^{k_i} + \sum_{j',\beta_{j'}=-1} P^{h_{j'}} = \sum_{i',\alpha_{i'}=-1} P^{k_{i'}} + \sum_{j,\beta_j=1} P^{h_j}. \tag{4}$$

However, the expressions on either side of this equation represent unique numbers in a P-base number system for $P \geqq 3$. These numbers may be designated by numbers having "1" in those positions where $k_i \neq h_j$, "2" where $k_i = h_j$, and zero elsewhere. Since $H \neq K$, however, the resulting numbers must differ in at least one place. The equality cannot, therefore, be satisfied. These results are restated as a theorem.

> Theorem: If the binary numbers corresponding to the canonical form of a logic function are interpreted as numbers of radix $P \geq 3$, a numerical difference of value
>
> $$\sum_{i=1}^{K} \alpha_i P^{k_i}, \qquad \alpha_i = \pm 1$$
>
> is a necessary and sufficient condition that the vertices are exactly K apart in n dimensional space.

While this theorem is applicable for any radix $P \geq 3$, greatest conciseness of notation is achieved by choosing a radix 3. This follows from the fact that the numbers

are to be recast into numerically equal decimal numbers. The largest number employed using a radix P with n independent variables will be $222 \cdots 2$, or

$$2 \sum_{j=0}^{n-1} P^j = \frac{2(P^n - 1)}{(P - 1)}.$$

If this number is recast into decimal notation the resulting number of digits is

$$x \doteq \log_{10} \frac{2(P^n - 1)}{(P - 1)}$$

or, for large n,

$$\frac{x}{n} \doteq \log_{10} P.$$

Hence, if a ternary radix is used, the number of decimal digits required is approximately 0.48 times the number of independent variables, while for a quaternary notation this ratio is 0.60.

Method for Determining Irredundant Coverings

Based on the work of Samson and Mueller [4–6], this ternary notation can be used to determine the irredundant coverings of a truth function. To do this it is necessary to determine for each vertex those cells which contain the vertex but are themselves not contained in a larger cell. Such cells will be called *basic*. To do this, first write all the vertices in ternary (binary) form, and then write the corresponding decimal numbers.

For a given vertex N, only those vertices whose vertex numbers are of the form $N \pm 3^h$ can form one-dimensional cells containing N. Now r one-dimensional cells define an r-dimensional cell provided all vertices of the form below are present.

$$N + \sum_{i=1}^{r} \alpha_i 3^{hi}, \qquad \alpha_i = \pm 1$$

Consider two vertices

$$N_1 = N + \alpha_i 3^{hi}$$
$$N_2 = N + \alpha_j 3^{hj}$$

which form one-dimensional cells with the vertex N. For these vertices, plus the vertex N, to form a two-dimensional cell, the vertex below must also be present.

$$N_{12} = N + \alpha_i 3^{hi} + \alpha_j 3^{hj}$$
$$N_{12} = N_1 + N_2 - N$$

For three vertices

$$N_1 = N + \alpha_i 3^{hi},$$
$$N_2 = N + \alpha_j 3^{hj},$$
$$N_3 = N + \alpha_k 3^{hk},$$

which form a one-dimensional cell with the vertex N to form a three-dimensional cell, the three two-dimensional cells requiring the additional vertices

$$N_{12} = N_1 + N_2 - N$$
$$N_{13} = N_1 + N_3 - N$$
$$N_{23} = N_2 + N_3 - N$$

must be present, as well as the vertex

$$N_{123} = N + \alpha_i 3^{hi} + \alpha_j 3^{hj} + \alpha_k 3^{hk}$$

or

$$N_{123} = N_{12} + N_3 - N$$
$$= N_{13} + N_2 - N$$
$$= N_{23} + N_1 - N.$$

This process is readily extended to higher order cells.

Consider a vertex which is embodied in only one basic cell. Such a basic cell is essential and must be present in any irredundant covering. Furthermore, the vertices embodied in this cell are thereby also covered and need not be separately considered. This results in a considerable decrease in the labor involved in determining an irredundant covering.

Consider those vertices which are not contained in a single basic cell. Tabulate these vertices together with the various basic cells in which they are embodied. If a larger cell covers the same vertices as a smaller cell, the smaller cell is not essential and may be deleted. If, as a result of this deletion, a vertex is now contained in only one remaining basic cell, this cell is essential.

The possible variations in the covering of the remaining vertices form the possible variations of the irredundant form. To form an irredundant covering containing the minimum number of cells, preference is given to those cells covering the largest number of the remaining vertices.

Example 1

The method will be applied to determine the irredundant form of a four-variable case. Consider the truthtable

0000, 0100, 0110, 0111, 1000, 1100, 1101, 1111

interpreted as numbers in ternary notation. The corresponding numbers in decimal notation are

0, 9, 12, 13, 27, 36, 37, 40.

To determine the basic cells embodying the vertices start with the vertex 0. For this vertex, the vertices of the form $0+3^2$ and $0+3^3$ are present, so that these vertices form one-dimensional cells with the vertex 0.

0 / 9 27 / .

Since there are two one-dimensional cells present, there is a possibility of a two-dimensional cell being present. This requires that the vertex $(9+27-0)$ or 36 be present. Since this vertex is present, these four vertices are embodied in a single two-dimensional cell. The numerical value of this cell is given by twice the largest vertex

minus the smallest or 72. Symbolically the process is written

$$0\ /\ 9\ 27\quad 36\ /(72.)$$

The circle about the cell number indicates that it is the only basic cell containing the vertex and hence is essential. The basic cells embodying 9, 27, and 36 need not be considered, although these vertices may be employed to simplify the cells about other vertices.

The remaining vertices form groups as follows

$$12\ /\ \ 9,\ \ 13\ /$$
$$13\ /\ 12,\ \ 40\ /$$
$$37\ /\ 36,\ \ 40\ /$$
$$40\ /\ 37,\ \ 13\ /.$$

Since no additional essential cells appear, the various possible coverings of the remaining vertices must be considered. To do this, list the vertices and the cells covering them.

Vertices	One-dimensional cells	
12	15	14
13	14	67
37	38	43
40	43	67

To find the irredundant coverings that employ the fewest possible cells, preference is given to those cells which cover the greatest number of vertices. Thus a minimum irredundant covering is

$$72 + 14 + 43.$$

Other irredundant coverings are found by covering each vertex at least once, with each cell covering at least one vertex not otherwise covered.

$$72 + \begin{cases} 15 + 67 + \begin{cases} 43 \\ 38 \end{cases} \\ 14 + 38 + 67. \end{cases}$$

If desired, these forms may be put into truthtable notation by converting the decimal numbers to a ternary notation. Thus, the minimum irredundant form becomes

$$2200 + 0112 + 1121$$

or

$$x_1'x_0' + x_3'x_2x_1 + x_3x_2x_0.$$

Example 2

The following example has seven variables and 43 terms in the canonical form. It is identical to the example described by Mueller [4], who generated it by reading modulo 128, the first 45 page numbers in an alphabetical index of a 2000-page volume. The entire calculation is shown below.

3, 10, 36, 93, 108, 109, 112, 117, 118, 120, 121, 243, 247, 253, 256, 280, 283, 325, 336, 351, 352, 354, 360, 361, 363, 729, 730, 732, 733, 739, 756, 760, 765, 810, 811, 849, 973, 975, 1000, 1002, 1008, 1054, 1065.

3 / 732 /(1461)

10 / 253 739 /

36 / 117 765 /

93 / 120 336 / 363 /(633)

108 / 109^a 117^b 351^c / 118^{ab} 352^{ac} 360^{bc} / 361^{abc} /(614)

112 / 109 121 / 118 /(133)

243 /(243)

247 / 256 /(265)

~~253 / 10^a 256^b 280^c / 283^{bc} /~~

~~280 / 283^a 253^b 361^c / 256^{ab} /~~

283 / 280 256 / 253 /(313)

325 / 352 1054 /

354 / 351 363 / 360 /(375)

739 / 730 10 /

729 / 730 732 756 810 / defer

730 / 729 733 739 973 811 / defer

733 / 732^a 730^b 760^c / 729^{ab} /

756 / 765 729 /

760 / 733 /(787)

765 / 756 1008 36 /

810 / 811 729 / 730 /(893)

849 / 120 /(1578)

973 / 1000^a 1054^b 730^c / 811^{bc} /

975 / 1002 732 /

1000 / 973 /(1027)

1002 / 975 /(1029)

1008 / 765 /(1251)

1054 / 973^a 811^b 325^c / 730^{ab} /

1065 / 336 /(1794.)

The calculation about those vertices embodied in many one-dimensional cells is deferred until the end because of the high probability that these vertices will appear in an essential cell. The calculation of the numerical value of the basic cells about a vertex that has more than one basic cell has also been deferred. This is done because these vertices may later appear in an essential cell and thus require no further consideration. Letter superscripts are employed, where necessary, to note what vertices are being considered.

Table I is formed by collecting those vertices not covered by essential cells.

TABLE I

Vertices	1-cells		2-cells
10	496	*1468*	
36	198	1494	
325	379	*1783*	
739	748	*1468*	
756	774	783	
1054	1783		1378

Smaller cells which are dominated by larger cells (in the sense that there is a larger cell which covers at least all those vertices covered by the smaller) are deleted. In this example the larger cell 1378 does not dominate 1783.

Various irredundant coverings are given by all of the essential cells plus those combinations of cells from this table which cover each vertex once. The minimum irredundant covering (in the sense of the least number of cells) is found by giving preference to those cells in this table which cover the largest number of vertices in this table. Thus 1468 and 1783 must be included in any minimum irredundant covering.

The irredundant coverings are given by the cells $133+243+265+213+375+614+633+787+893+1027+1029+1251+1461+1578+1794$ and

$$+\begin{Bmatrix}198\\1494\end{Bmatrix}+\begin{Bmatrix}774\\783\end{Bmatrix}+\begin{cases}1468+1783 \leftarrow \text{minimum}\\1468+1378+379\\496+748+1783\\496+748+1378+379.\end{cases}$$

In conventional truthtable notation the minimum irredundant forms are

133	0 0 1 1 – – 1
243	0 1 0 0 0 0 0
265	0 1 0 0 – 1 1
313	0 1 0 – 1 – 1
375	0 1 1 1 – – 0
614	0 – 1 1 – 0 –
633	0 – 1 – 1 1 0
787	1 0 0 – 0 1 1
893	1 0 – 0 0 0 –
1027	1 1 0 – 0 0 1
1029	1 1 0 – 0 1 0
1251	1 – 0 1 1 0 0
1461	– 0 0 0 0 1 0
1468	– 0 0 0 1 0 1
1578	– 0 1 1 1 1 0
1783	– 1 1 0 0 0 1
1794	– 1 1 0 1 1 0
198 or 1494	00 – 1100 or – 001100
774 or 783	1001 – 00 or 100 – 00.

Alternate Procedures

It is possible to develop an alternate procedure wherein the ternary one and two are interchanged. The number designating a particular cell is then simply the average value of the numbers representing the vertices. While this coding has some elegance, it is nevertheless more work to average several numbers than to perform the operation of "twice the largest minus the smallest."

In some instances it may be desirable to perform operations directly with the cells. The following theorem is then of interest.

Theorem: If the binary numbers corresponding to the canonical form of a logic function are interpreted as numbers of radix $P \geq 4$ and the corresponding cells are designated by the proper locations of the digit two for those variables not required to describe the cell, then the necessary and sufficient condition that two r-dimensional cells form a larger $(r+1)$ cell is that the difference of their corresponding r-cell numbers be of the form P^h. The proper $(r+1)$-cell number is then given by twice the larger r-cell number minus the smaller.

When a radix 3 is used, it is possible to have two r cells with a difference of 3^h which have an $(r-1)$ cell in common. Such r cells effectively form a "corner" of the n-dimensional cell and are thus not combinable into an $(r+1)$ cell unless the appropriate additional $(r-1)$ cell is present.

This theorem permits the entire cell structure of a truth function to be calculated and displayed in compact form. While it is possible to utilize a radix 3, the additional precautions required appear to make a radix 4 more desirable.

Example 3

The vertices chosen for example 1 will be again utilized, but now the entire cell structure instead of just the minimum form will be determined.

The corresponding decimal numbers of the vertices, using a radix 4, are

0, 16, 20, 21, 64, 80, 81, 85.

The results of the calculation are shown in Table II.

TABLE II

Vertices	1-cells		2-cells	
0	32	128		160
16	32	24	144	160
20	22	24		
21	22	149		
64	96	128		160
80	96	82	144	160
81	89	82		
85	89	149		

Calculation of the 2-cells requires searching the list of 1-cells. This constitutes one of the main disadvantages of the method because the 1-cells are not in numerical order. However, the main advantage is that the cell structure of the truth function is directly displayed.

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Computing Techniques for the Sampling Parametric Computer*

C. J. HIRSCH† AND F. C. HALLDEN†

Summary—**This paper describes novel calculating techniques suitable for an electronic analog computer using exponential discharges to simulate the logarithmic scales of the slide rule. Among others, the device can perform the following operations: $z=xy$; $z=x/y$; $z=xy^a$; $\log_a x$; a^x; and evaluate such series as $y=Ax^a+Bx^b+Cx^c+\cdots$ where the exponents can be fractional and z, x, and y can be time variables. The problems can be solved explicitly or implicitly; thus in the above series y (or x) can be determined with equal ease if x (or y) are given. The Appendix describes an actual computer which gave accuracies of 1 to 2 per cent of full range from 0 to 95 per cent of full range and 4 per cent from 95 to 100 per cent of full range without recalibration for different groups of problems. The accuracy can be increased by calibrating the device for a specific group of problems.**

History

THE COMPUTING techniques described in this paper were originally developed for a RHO-THETA navigational electronic analog computer using distance measuring equipment (dme) to obtain distance (RHO) and a VOR receiver to obtain bearing (THETA). The distance information is supplied by the dme as a dc voltage whose value is proportional to distance. A computer capable of handling this data directly was then developed. Since its original concept the computer has been greatly expanded and diversified. It has been used for navigation, equation solving, the generation of unusual mathematical functions, and fire control problems.

Introduction

This paper describes calculating techniques which are suitable for a novel type of electronic analog computer known as the sampling parametric computer. These techniques permit computations according to all the operations of algebra and, in addition, provide simple means for certain calculations which heretofore have not been conveniently performed. Among the latter are the evaluation of power and transcendental series and the solution of higher-degree equations whose exponents need not be integers. The computer operating with these techniques provides the convenient generation of many of those functions which can be expanded into series.

For example, the computer uses circuits which can calculate y or x with equal ease in the equation,

$$y = Ax^a + Bx^b + Cx^c + \cdots$$

(where x and y are variable functions of time and a, b, c, etc. need not be integers).

Since this computer can use fractional exponents, it can compress long series into only a few terms which closely approximate the function and require only simple circuitry to implement, such as

$$\sin x \cong x - x^{2.9}/6.44.$$

It can calculate more complicated functions with more elaborate circuits.

As used here, an electronic analog computer is one that performs mathematical operations on physical quantities whose magnitudes are expressed in electrical analogs, such as volts per mile, volts per kilogram, etc. In addition, the analog computer handles magnitudes expressed in terms of the complete class of real numbers, integers and fractions. While less accurate than the digital machines, its simplicity of programming and

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rapidity of operation make it desirable for many problems of control and computation for which large digital machines are cumbersome. The sampling parametric computer utilizes inputs expressed as voltage analogs. It carries out the computation by electrical means, and its output is a voltage which is an analog representation of the magnitude of the physical quantity desired.

The techniques described here are similar to the repeated observation of a slide rule and the circuits involved are electrical analogs of the scales and indicators of the slide rule. The magnitudes engraved on the different scales of the slide rule can be expressed by simultaneous equations in terms of the common *parameter of distance* along the scale. The computing techniques described in this paper similarly make use of magnitude scales which are disposed in time, instead of distance, and can be expressed by simultaneous equations in terms of the common *parameter of time.*

The quantities used in most control operations vary with time. Computations involving such variables are performed by rapid repetition of the computation on instantaneous values of the variable which are assumed to be constant during each computation. As soon as the computation is completed, the process is repeated on a new *sample* of the variable. Hence the name sampling parametric computer.

Principle of Operation

The principle of operation will be made clearer by examining the process of division, $z=y/w$, which is illustrated in Fig. 1(a). Specifically we shall compute $48/16=3$, a very simple example which will allow checking the validity of the process. The independent variables y and w are expressed as analog voltages $E_y=48$v and $E_w=16$v which are caused to charge respectively two capacitors C_y and C_w, having equal capacitance C, through switches S_y and S_w. At a given instant $t=0$, the two switches are opened simultaneously causing the charges on C_y and C_w to discharge respectively through two equal resistors of value R. The voltages on these capacitors decay exponentially as shown in Fig. 1(b), and their instantaneous values e_w and e_y, are respectively

$$e_w = E_w\epsilon^{-t/RC} \tag{1}$$

$$e_y = E_y\epsilon^{-t/RC}. \tag{2}$$

The first of these, e_w, reaches the value E_x at the instant t_1 when, simultaneously, e_y reaches the value E_z so that

$$E_x = E_w\epsilon^{-t_1/RC} \tag{3}$$

$$E_z = E_y\epsilon^{-t_1/RC}. \tag{4}$$

The relations among E_x, E_w, E_z, and E_y established by the rundown process can be examined by dividing (4) by (3), which results in

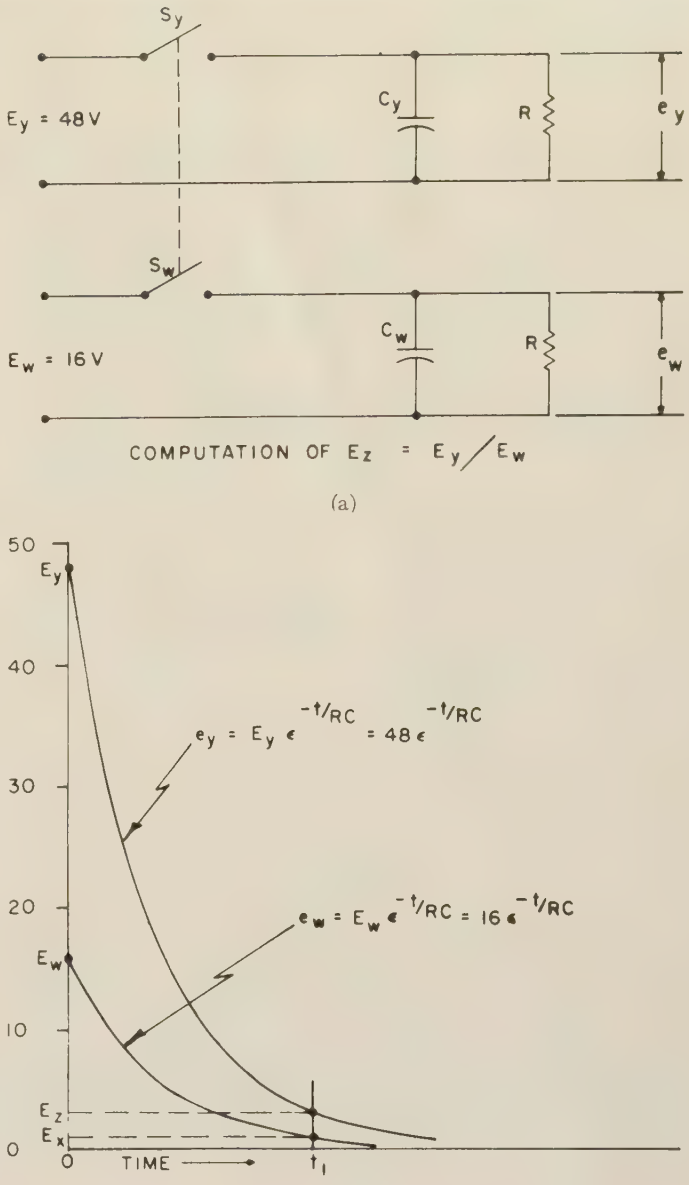


Fig. 1.

$$E_z = \frac{E_y}{E_w}E_x. \tag{5}$$

If E_x is made equal to unity in the scale used for all voltages, the answer is

$$E_z = E_y/E_w \quad \text{or, by analogy,} \quad z = y/w.$$

For the numerical example given above, Fig. 1(b) shows that e_y reaches the value $e_y=E_z=3$ v at the instant that $e_w=E_x=1$ v. The answer is $E_z=3$ v. The computer requires a device to measure E_z at the instant that $e_w=1$ v.

The analogy to the slide rule is apparent. To divide 48 by 16, magnitudes corresponding to 48 and 16 are lined up opposite each other on the D and C scales respectively of the slide rule. The scales vary logarithmi-

cally from this point and the answer $48/16=3$ is read on scale E at the value corresponding to unity on scale C.

The computer operates on variables by repeating the process of solution for successive values of the independent variable. Successive solutions can be reinserted into the problem to synthesize answers to special problems. Thus integration is performed by storing the sum of successive values of the function to be integrated. Differentiation is performed by successively subtracting the value of the function at one instant from its value after a fixed increment of time.

Although means of solving many problems will suggest themselves, the following examples are illustrated:

1) $z=w(x/y)^n$. This relation is used for multiplication, division, and powers.
2) $z=\log_a x$, and $x=a^z$.
3) $z=Ax^a+Bx^b+Cx^c+\cdots$. This relation can be used to generate, or find the roots of, functions which can be expressed in series form.
4) $z=\int_0^t x\,dt$ and $\int_0^y x\,dy$.
5) $z=dx/dt$ and dx/dy.

The exponents in 1) and 3) need not be integers but should be real. Quantities z, w, x, and y can be variable functions of time.

Instrumentation

In addition to the actual generation of the auxiliary functions, which correspond to the scales of a slide rule and which may obey the appropriate mathematical laws desired, the computer uses three special devices called 1) a comparator, 2) a sampling switch, and 3) a solution iterative switch. The operation of these devices is symbolized in Fig. 2. A practical form is detailed in the Appendix.

1) Comparator

This device is shown as K in Fig. 2(a). Its purpose is to recognize the instant t_1 when a scanning voltage E_s, applied at point 1 is just equal to the data voltage E_d applied at point 2. At that instant a marking signal appears at point 3. The marking signal usually acts to trigger the sampling switch.

2) Sampling Switch

This device is shown as SS in Fig. 2(a). Switch SS closes for an instant Δt whenever $E_s=E_d$. The time relations relating K and SS are shown by the graphs of Fig. 2(a).

3) Solution Iterative Switch

This is shown as SIS in Fig. 2(b). Its purposes are a) by closing to place the various circuits into operating condition by allowing suitable capacitors to be charged, b) to open and thereby initiate the solution by causing

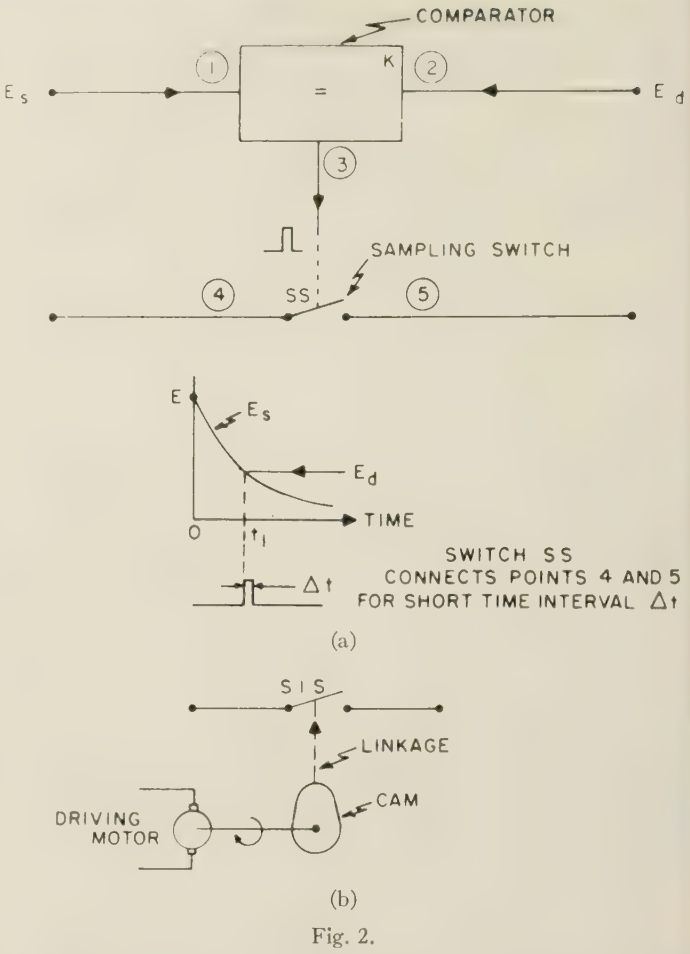


Fig. 2.

the discharge of capacitors, c) to remain open during the solution, and d) to close to place the various circuits in condition to repeat the solution. Although the "solution iterative switch" is symbolized for simplicity by a cam-operated mechanical switch, an all-electronic equivalent is usually preferred.

Solution of $z=w(x/y)^n$

As a first illustration of the operation of this computer, suppose that it is desired to solve $z=w(x/y)^n$, where n is a known constant, usually not an integer, and z, w, x, and y may be variables. This particular problem is chosen because it combines multiplication, division, and raising to a power, and is conveniently handled by the computer.

$$z = w(x/y)^n. \tag{1}$$

The first step in the solution is to assign analog voltages E_w, E_x, and E_y which are proportional to the independent variables w, x, and y. The answer z will appear as an analog voltage E_z proportional to z.

These voltages are applied as shown to the circuit of Fig. 3(a) in which capacitors C_1 and C_2 and resistors R_1 and R_2 are related by

$$C_1R_1/C_2R_2 = n. \tag{2}$$

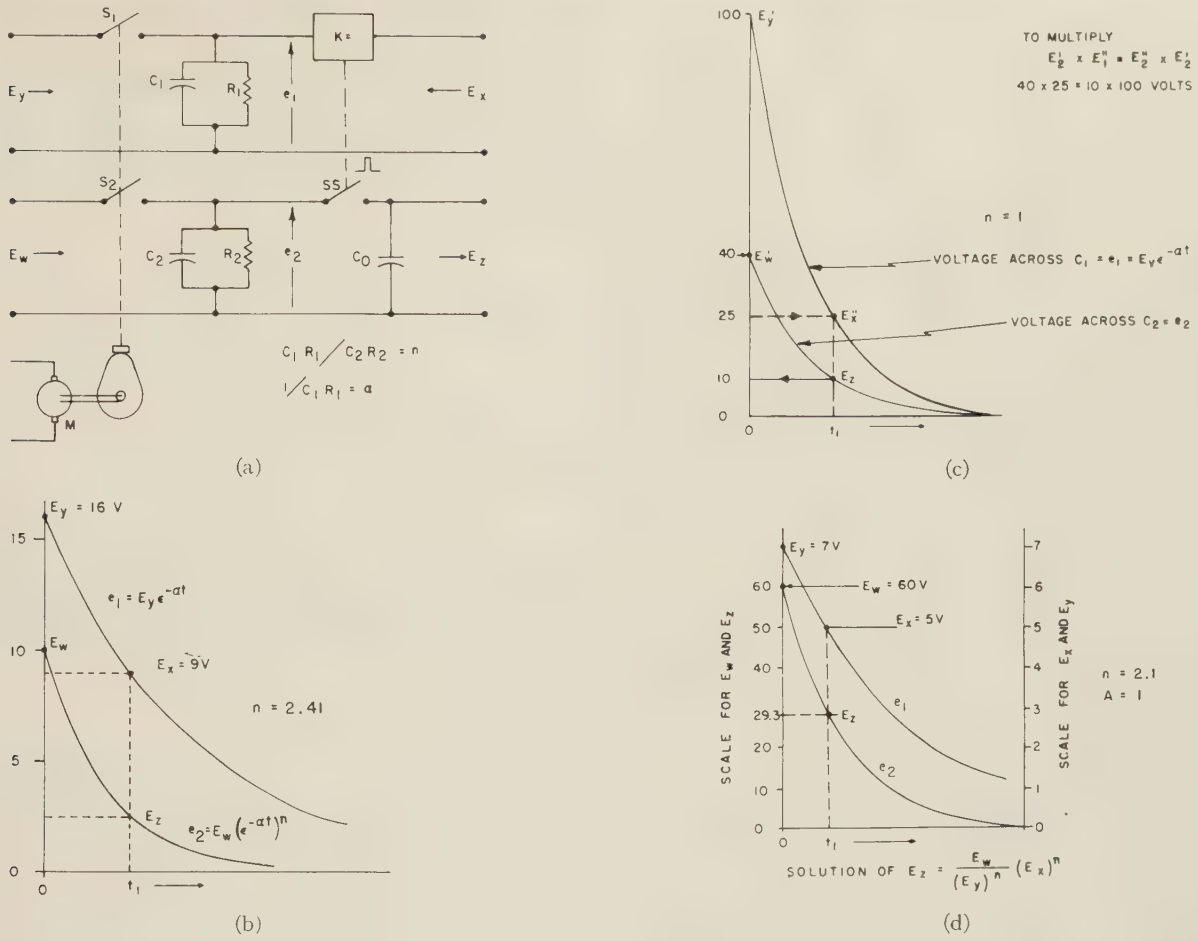


Fig. 3.

Switches S_1 and S_2 are closed to charge C_1 and C_2 to E_y and E_w, respectively. These switches are then opened simultaneously, causing the charges on C_1 and C_2 to leak through R_1 and R_2. The instantaneous voltages e_1 and e_2 on C_1 and C_2 decay exponentially according to the time constants

$$C_1R_1 = 1/\alpha \tag{3}$$

$$C_2R_2 = 1/n\alpha \tag{4}$$

as shown in Fig. 3(b), so that

$$e_1 = E_y\epsilon^{-\alpha t} \tag{5}$$

and

$$e_2 = E_w\epsilon^{-n\alpha t} = E_w(\epsilon^{-\alpha t})^n. \tag{6}$$

Voltage e_1 reaches the value E_x at time t_1, so that

$$e_1 = E_x = E_y\epsilon^{-\alpha t_1} \tag{7}$$

or

$$\epsilon^{-\alpha t_1} = E_x/E_y. \tag{8}$$

The comparator K recognizes the instant t_1 (when $e_1 = E_x$) and causes the sampling switch SS to close for a short time and immediately reopen thus trapping the value of e_2 at time t_1 on capacitor C_0. This value of e_2 is called E_z.

At this instant

$$e_2 = E_w(\epsilon^{-\alpha t_1})^n = E_z. \tag{9}$$

Substituting (8), $(\epsilon^{-\alpha t_1} = E_x/E_y)$, in (9),

$$e_2 = E_2 = E_w\left(\frac{E_x}{E_y}\right)^n \tag{10}$$

since E_w, E_x, E_y, and E_z are proportional to w, x, y, and z, respectively,

$$z = w(x/y)^n. \tag{1}$$

After each solution, switches S_1 and S_2 are closed, by motion of the cam M, to repeat the cycle of solution for new values of w, x, and y.

To illustrate the process of solution, numerical values are assigned in Fig. 3(b) to $E_w = 10$ v, $E_y = 16$ v, $E_x = 9$ v, and $n = 2.41$. In the time required for e_1 to decay from 16 v to 9 v, e_2 has decayed from 10 v to 2.5 v, which is

$$10(9/16)^{2.41} = 2.5 \text{ v}.$$

Multiplication

For this computation the general equation $z = w(x/y)^n$ is changed to

$$zy = wx \tag{11}$$

by making $n = C_1R_1/C_2R_2 = 1$. w is the multiplicand, x is the multiplier, and z is the answer which must be multiplied by a constant y to give the absolute value. The value of y can be made equal to unity if desired. Figs. 3(a) and 3(c) illustrate a numerical example for which $w = 40$ and $x = 25$.

Capacitor C_1 is charged through S_1 to a value of E_y which is larger than $E_x = 25$ v, because the voltage e_1, on C_1, must decay to 25 v. E_y should be chosen also for its convenient use as a factor. The value $E_y = 100$ v satisfies these conditions. Capacitor C_2 is charged to $E_w = 40$ v through S_2. Discharge of C_1 and C_2 is simultaneously initiated at time $t = 0$ by opening S_1 and S_2.

When [Fig. 3(c)] $e_1 = E_y\epsilon^{-\alpha t_1} = 100\epsilon^{-\alpha t_1}$ v reaches equality with $E_x = 25$ v, at the time t_1, the comparator K operates the sampling switch SS to trap the instantaneous value of e_2 (at t_1) which is found to be equal to 10 v as shown below.

At $t = t_1$, $e_1 = E_y\epsilon^{-\alpha t_1} = E_x = 25$ so that

$$\epsilon^{-\alpha t_1} = \frac{E_x}{E_y} = \frac{25}{100} = 0.25. \tag{12}$$

Also,

$$e_2 = E_z = E_w\epsilon^{-\alpha t_1} = \frac{E_wE_x}{E_y} = \frac{40 \times 25}{100} = 10 \text{ v}.$$

This value of $E_z = 10$ v is then multiplied by the scale factor $E_y = 100$ v to give the correct absolute answer of 1000.

Division

Division has already been described in the introduction.

Powers and Roots of Variables

For this problem the general equation $z = w(x/y)^n$ is rewritten as $z = (w/y^n)x^n$, where

$$\frac{w}{y^n} = A. \tag{13}$$

Quantity A is a scale factor which is usually made equal to unity or some other convenient value. In the following example $A = 1$.

As a numerical example compute $z = 5^{2.1}$. The structure is shown in Fig. 3(a) for which $E_x = 5$ v and $n = 2.1$. The value of E_y is chosen to be greater than $E_x = 5$ v but not so great as to make $E_y^{2.1}$ excessive; a suitable value is $E_y = 7$ v making $E_y^{2.1} = E_w = 7^{2.1} = 60$ v. The time constants are adjusted in the ratio of $C_1R_1/C_2R_2 = n = 2.1$.

Referring to Fig. 3(d) in time required for $e_1 = E_y\epsilon^{-\alpha t}$ to decay from $E_y = 7$ v to $E_x = 5$ v, $e_2 = E_w(\epsilon^{-\alpha t_1})^n$ has decayed from 60 v to 29.3 v which is $E_z = 5^{2.1} = 29.3$ v.

Note that it is just as practical to find the 2.1 root of 29.3,

$$29.3^{1/2.1} = 5$$

by sampling e_1 when $e_2 = 29.3$ v.

Logs and Antilogs of Variables

For these relations we write

$$z = \log_a x \tag{14}$$

and

$$x = a^z. \tag{14a}$$

To evaluate $z = \log_a x$, a decaying exponential $e_1 = E_y\epsilon^{-\alpha t}$ is started simultaneously with a decreasing sawtooth $e_2 = E_w - kt$ as shown in Fig. 4. Voltages e_1 and

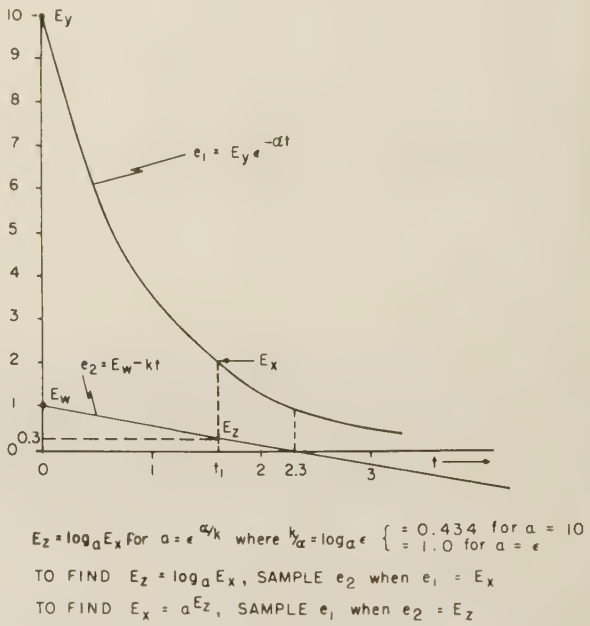


Fig. 4.

e_2 simultaneously reach E_x and E_z respectively at time t_1. This is expressed as

$$e_1 = E_x = E_y\epsilon^{-\alpha t_1} \tag{15}$$

and

$$e_2 = E_z = E_w - kt_1. \tag{16}$$

From (15)

$$\epsilon^{-\alpha t_1} = E_x/E_y$$

so that

$$t_1 = -\frac{1}{\alpha}\log_\epsilon \frac{E_x}{E_y}. \tag{17}$$

Substituting this value in e_2 (16)

$$e_2 = E_z = E_w + \frac{k}{\alpha}\log_\epsilon \frac{E_x}{E_y} \tag{18}$$

$$= E_w + \frac{k}{\alpha}\log_\epsilon E_x - \frac{k}{\alpha}\log_\epsilon E_y. \tag{19}$$

Let

$$E_w - \frac{k}{\alpha}\log_\epsilon E_y = 0. \tag{20}$$

Then

$$e_2 = E_z \doteq \frac{k}{\alpha}\log_\epsilon E_x. \tag{21}$$

From the standard mathematical formula,

$$\log_a x = \log_a \epsilon \log_\epsilon x \tag{22}$$

it is seen that E_2 can be made equal to $\log_a x$ by setting

$$\frac{k}{\alpha} = \log_a \epsilon. \tag{23}$$

For logarithms to the base 10, $k/\alpha = 0.434$.

Referring to (20),

$$E_w - \frac{k}{\alpha}\log_\epsilon E_y = 0 \tag{20}$$

can be rewritten as

$$E_w - \log_a \epsilon \log_\epsilon E_y = E_w - \log_a E_y = 0$$

so that

$$E_w = \log_a E_y. \tag{24}$$

Therefore in Fig. 4, the initial amplitude of the sawtooth (16) is made equal to the logarithm of the maximum value of the independent variable E_x. The slope k of the sawtooth is adjusted so that it is equal to the time constant (α) of the exponential multiplied by $\log_a \epsilon$ (23). This last condition can be expressed also by saying that the sawtooth is equal to zero ($e_2 = 0$) at the instant that $e_1 = 1$.

It should be noted that the base of the logarithms can be changed by altering E_w and k. It should also be noted that

$$x = a^z \tag{14a}$$

can be measured equally well by sampling e_1 at the instant that $e_2 = E_z$.

The numerical example in Fig. 4 illustrates the principle for obtaining common logarithms ($a = 10$) for values of $x \leqq 10$. The initial value of the sawtooth at $t = 0$ is equal to $E_w = \log_{10} 10 = 1$. It is equal to zero when $e_1 = 1$. For example, the value of $\log_{10} 2$ is seen to be 0.3. Other values may be checked.

General Evaluation and Solution of Power Series

The process previously described of raising a variable to a given power ($z = Ax^n$) can be extended to generate many functions which can be expressed as power series of an independent variable, such as

$$z = Ax^a + Bx^b + Cx^c + \cdots. \tag{25}$$

The method also affords the solution of power equations. Thus (25) can be solved for x as well as z. The exponents (a, b, c, etc.) to which the variable x is raised need not be integers. As stated in the introduction, this often allows the use of more rapidly converging series, which require fewer terms for the required accuracy, than would be the case if only integers could be used. For example, if only the first two terms of the series

$$\sin x = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \cdots \tag{26}$$

are taken, the series will be in error by as much as 7.7 per cent in the range $0 < x < \pi/2$ radians.

If, however, it is modified to

$$\sin x \simeq x - \frac{x^{2.9}}{6.44} \tag{27}$$

the maximum error is only 0.52 per cent over the same range. The instrumentation for (27) will be discussed after the general case of (25) is demonstrated.

Another advantage of the ability to use nonintegral exponents is that it greatly facilitates the experimental adjustment of the computer to fit a given curve. Once the curve is fitted, the computer can generate instantaneous values of the function for instantaneous values of the independent variable or, vice versa, often solve for the independent variable for instantaneous values of the function. The ability to solve such series is believed to be much easier than with earlier types of computers.

Evaluation and Solution of $z = Ax^a + Bx^b + Cx^c + \cdots$

Fig. 5 shows a block diagram of the arrangement to evaluate z in this case.

When the switch S_1 is closed, C_x is charged to the value E_y and C_a, C_b, C_c, etc. are charged respectively to iR_a, iR_b, iR_c, etc. When the switch S_1 is opened C_x discharges through R_x so that the voltage e_1 across C_x is

$$e_1 = E_y \epsilon^{-t/R_x C_x}. \tag{28}$$

Similarly the voltages across C_a, C_b, C_c, etc.

$$e_a = iR_a \epsilon^{-t/R_a C_a}$$

$$e_b = iR_b \epsilon^{-t/R_b C_b}.$$

Since R_aC_a, R_bC_b, R_cC_c, etc. are in series the voltage e_2, across the chain, is

$$e_2 = iR_a \epsilon^{-t/R_a C_a} \pm iR_b \epsilon^{-t/R_b C_b} + iR_c \epsilon^{-t/R_c C_c} + \cdots. \tag{29}$$

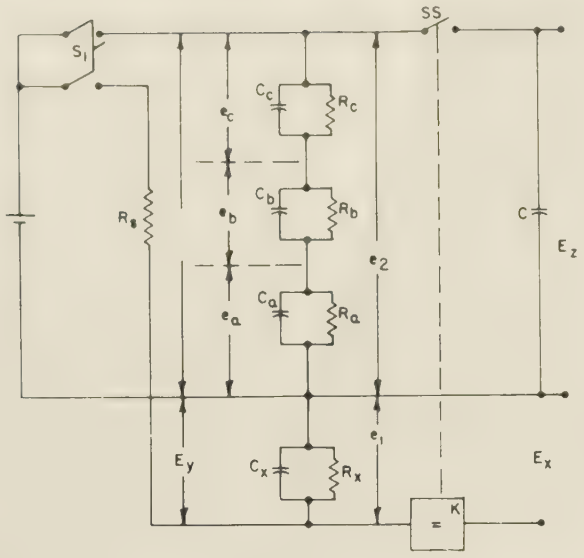


Fig. 5.

Let

$$R_xC_x = aR_aC_a = bR_bC_b = cR_cC_c. \tag{30}$$

Substituting these values in (29)

$$\begin{aligned} e_2 &= iR_a\epsilon^{-at/R_xC_x} + iR_b\epsilon^{-bt/R_xC_x} + iR_c\epsilon^{-ct/R_xC_x} + \cdots \\ &= iR_a(\epsilon^{-t/R_xC_x})^a + iR_b(\epsilon^{-t/R_xC_x})^b \\ &\quad + iR_c(\epsilon^{-t/R_xC_x})^c + \cdots. \end{aligned} \tag{31}$$

The voltage e_1, across C_x reaches the value E_x at the time t_1 or,

$$e_1 = E_x = E_y\epsilon^{-t_1/R_xC_x}$$

which gives

$$\epsilon^{-t_1/R_xC_x} = E_x/E_y. \tag{32}$$

At this instant (t_1) the comparator K closes the sampling switch SS momentarily thus trapping on capacitor C the value of e_2 at time t_1.

At time t_1, e_2 has reached the value E_z so that substituting $t=t_1$ and (32) in the value for e_2 given in (31),

$$\begin{aligned} e_2 = E_z &= iR_a\left(\frac{E_x}{E_y}\right)^a + iR_b\left(\frac{E_x}{E_y}\right)^b \\ &\quad + iR_c\left(\frac{E_x}{E_y}\right)^c + \cdots \end{aligned} \tag{33}$$

which can be rewritten as

$$e_2 = E_z = \frac{iR_a}{E_y{}^a}E_x{}^a + \frac{iR_b}{E_y{}^b}E_x{}^b + \frac{iR_c}{E_y{}^c}E_x{}^c + \cdots. \tag{34}$$

This equation is seen to be the electrical analog to

$$z = Ax^a + Bx^b + Cx^c + \cdots \tag{25}$$

where

$$\begin{aligned} A &= \frac{iR_a}{E_y{}^a}, \qquad B = \frac{iR_b}{E_y{}^b}, \\ C &= \frac{iR_c}{E_y{}^c}, \cdots M = \frac{iR_m}{E_y{}^m}. \end{aligned} \tag{35}$$

The structure described above evaluates z in (25) when x is known. It is obvious that, by interchanging the comparator K and the sampling switch SS, it is possible to solve for x when z is given.

Negative coefficients can be introduced by charging the proper capacitor with a battery having the opposite polarity, by using an inductor-resistor combination and placing a secondary winding on the inductor, which secondary can be poled to either polarity, or by special artifice such as is shown in Fig. 6 and described in the next section.

Example -To Compute $z=\sin x$, and $x=\arcsin z$

As discussed above,

$$\sin x \simeq x - x^{2.9}/6.44. \tag{27}$$

The circuit for this computation is shown in Fig. 6(a). When the switch S at the upper left is closed, battery V charges C_1 and C_2 to voltages iR_1 and iR_3, respectively. Opening the switch will cause the voltages e_1 across R_1 to decay according to

$$e_1 = iR_1\epsilon^{-t/R_1C_1} = E_y\epsilon^{-\alpha t}.$$

Likewise on opening switch S, the voltage across C_2, which is equal to iR_3, divides between R_2 and R_3 in such a manner that the portion across R_2 is equal to $-iR_2R_3/(R_2+R_3)$. Note that the current flows from R_2 into C_2, hence the negative sign.

As shown in Fig. 6(b), the voltage e_2, across R_2, will decay according to

$$e_2 = -i\frac{R_2R_3}{R_2+R_3}\epsilon^{-t/(R_2+R_3)C_2}$$

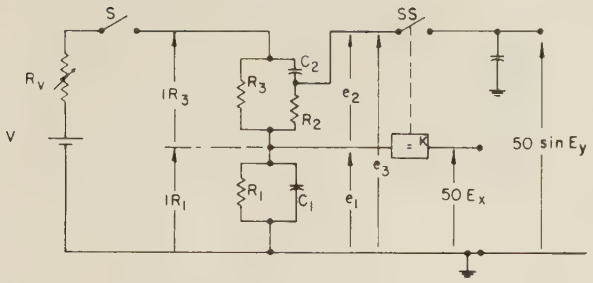
so that the sum e_1+e_2 is

$$e_3 = e_1 + e_2 = iR_1\epsilon^{-t/R_1C_1} - i\frac{R_2R_3}{R_2+R_3}\epsilon^{-t/(R_2+R_3)C_2}. \tag{36}$$

At time $t=t_1$, e_1 decays to the value E_x which is the analog of x so that it must start from a value $E_y=iR_1$ which is higher than the maximum value of x. Since this was taken as $x_{\max}=\pi/2$, $E_y=2$ v is a convenient value.

Writing (27) in analog form with

$$\begin{aligned} \sin E_x &= E_x - E_x{}^{2.9}/6.44 \\ &= 2\epsilon^{-\alpha t_1} - (2\epsilon^{-\alpha t_1})^{2.9}/6.44 \\ &= 2\epsilon^{-\alpha t_1} - 1.16\epsilon^{-2.9\alpha t_1}. \end{aligned} \tag{37}$$

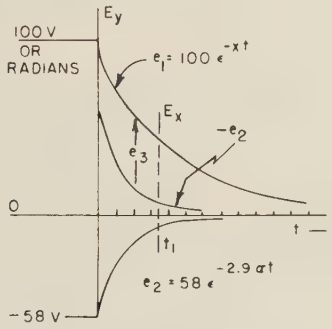


IR_1 = 100 VOLTS MAX

$IR_3 = 58(R_2 + R_3)/R_2$ VOLTS MAX

$R_1 C_1/(R_2+R_3) C_2 = 2.9$

(a)



INSTRUMENTATION TO COMPUTE

$50 \sin x \simeq 50x - 50x^{2.9/6.44}$ FOR $0 < x < \pi/2$

$\simeq 100\epsilon^{-\alpha t_1} - 58\epsilon^{-2.9\alpha t_1}$

(b)

Fig. 6.

Because the comparator described in the Appendix operates best with higher voltages than those in the range 0–1 v, the scale of (37) is changed by multiplying the whole equation by some convenient factor such as 50. This equation then becomes

$$50 \sin E_x = 50(2\epsilon^{-\alpha t_1}) - 50(1.16\epsilon^{-2.9\alpha t_1}) = 100\epsilon^{-\alpha t_1} - 58\epsilon^{-2.9\alpha t_1} \quad (38)$$

To implement this equation, the constants in Fig. 6(a) are adjusted as follows:

1) iR_1 and $iR_2R_3/(R_2+R_3)$ are made respectively equal to 100 v and 58 v.
2) The time constant $1/(R_2+R_3)C_2$ is made equal to $2.9/R_1C_1$.

Then when the switch is opened, the voltage e_1 on C_1 decays according to $e_1 = 100\epsilon^{-\alpha t}$ and reaches the value E_x at time t_1 so that

$$E_x = 100\epsilon^{-\alpha t_1}.$$

At the same instant ($t = t_1$), e_3 has reached the value given in (38). The comparator K causes the sampling switch SS to close momentarily causing the value 50 sin E_x to be trapped on C_0.

To compute $x = \arcsin z$, the comparator K and the sampling switch are interchanged.

Integration

Integration with respect to time is performed by adding successive values of the independent variable which are spaced by equal increments of time. An extension of the method which allows integration with respect to another variable is discussed in a later section.

Function $e(t)$ to be integrated with respect to time from t_1 to t_2, shown in Fig. 7(b), next page, is impressed across terminals 1, 2 of the circuit of Fig. 7(a). A source of periodic voltage preferably linear but expressed for convenience here as $E_0 \sin wt$ is produced by transformer T across terminals 4, 5. Voltage $E_0 \sin wt$, in Fig. 7 (b), is made greater in amplitude than the voltage across terminals 2, 3 of Figs. 7(a) or 7(c),

$$\int_{t_1}^{t_2} e(t)dt$$

and $w/2\pi$ is made higher than the highest frequency in $e(t)$. Assume for simplicity that the initial charge on C is zero.

As $E_0 \sin wt$ increases, it reaches a value at time t_1 when it is equal to $e(t_1)$ plus the voltage on C (which is assumed for convenience to be initially zero). At that instant $E_0 \sin wt_1 = e(t_1)$. The comparator K closes the sampling switch SS for a short time which is long enough to charge C to the value $e(t_1)$. The voltage $e(t_1)$ is trapped on C by the opening of the sampling switch. During the next cycle, $E_0 \sin wt$ reaches a value, at time t_2, when it is just equal to the voltage $e(t_1)$ stored on the capacitor plus the new value of $e(t)$ at the time t_2 so that

$$E_0 \sin wt_2 = e(t_1) + e(t_2).$$

The comparator again closes the sampling switch long enough to charge C to this value. The switch then opens, trapping this value on the capacitor. It is obvious that after n cycles, the voltage on C will be

$$E_0 \sin wt_n = e(t_1) + e(t_2) + \cdots + e(t_n). \quad (39)$$

Since the intervals Δt between samples can be made very nearly equal we can write

$$E_c\Delta t = \sum_1^n e(t)\Delta t$$

and if the samples are made very frequently

$$E_c\Delta t = \sum_1^n e(t)\Delta t \simeq \int_{t=0}^{t} e(t)dt. \quad (40)$$

While the intervals Δt are not strictly equal to each other they can be made very nearly so by making $E_0 \sin wt$ rise very steeply.

The capacitor C can even have appreciable leakage, as the charge on it is restored after each cycle and the leakage from C can be compensated by charging C each

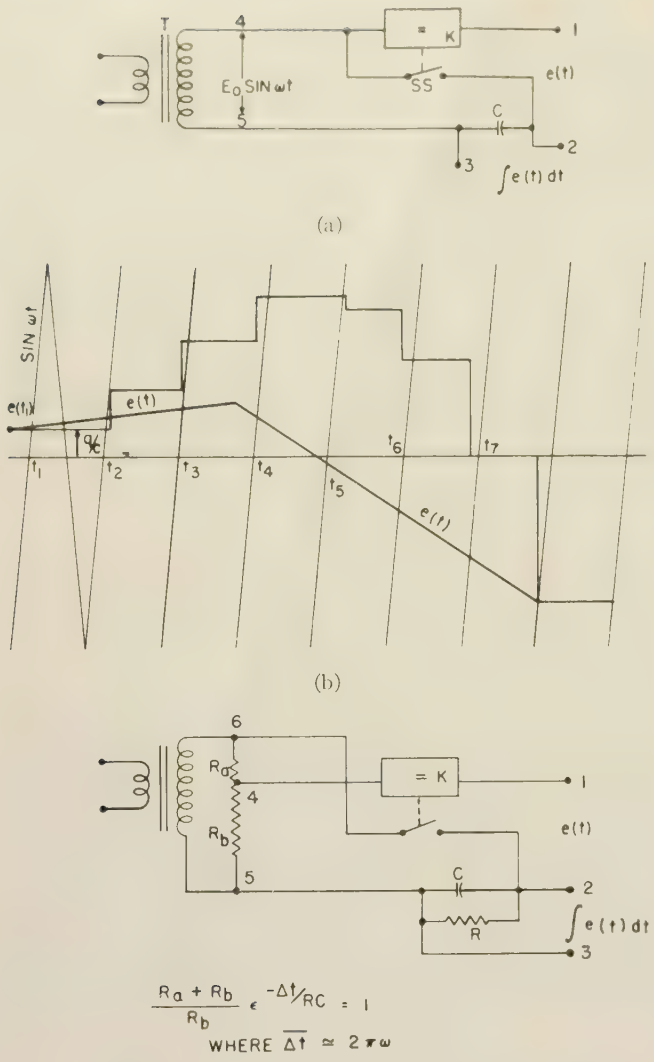


Fig. 7.

time from a voltage just great enough to compensate for the leakage. Thus if C is shunted by R, the voltage on it would be reduced to

$$E_c\epsilon^{-\Delta t/RC}$$

after the interval Δt. Since Δt is the interval between cycles its value is well known. The voltage applied to the capacitor is therefore increased by a factor M such that

$$M\epsilon^{-\Delta t/RC} = 1$$

as shown in Fig. 7(c).

Differentiation

The circuit for differentiation is shown in Fig. 8(a) and its operation is shown in the waveform diagram of Fig. 8(b). The circuit samples the function to be differentiated $e(t)$ at regular intervals. The value of the function at these times is written $e(t_n)$, $e(t_{n-1})$, etc. The value of the function at time (t_{n-1}) is stored so as to subtract it from its value at the time t_n. The difference

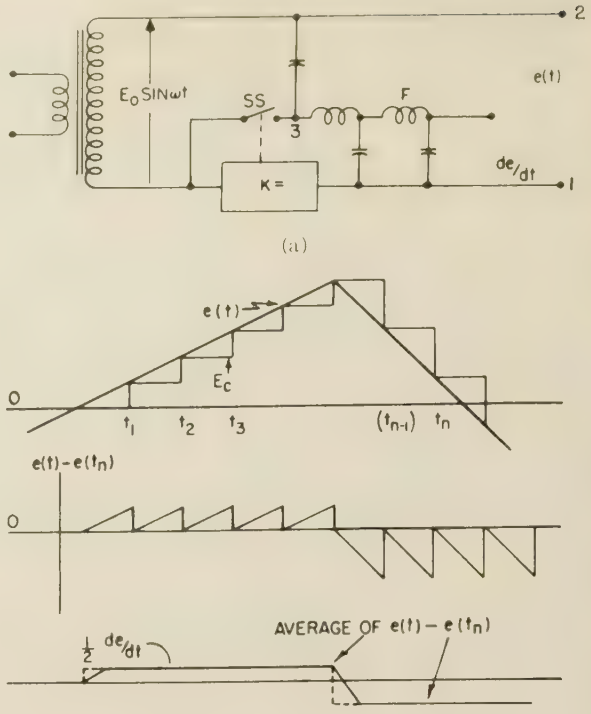


Fig. 8.

$e(t_n) - e(t_{n-1})$ between intervals is proportional to the derivative $de(t)/dt$.

Referring now to Fig. 8(a), whenever $E_0 \sin wt = e(t)$ at times t_1, t_2, t_{n-1}, t_n, the comparator K closes the sampling switch SS for a short interval of time during which capacitor C is charged to the value of $e(t_n)$ as shown by curve E_c of Fig. 8(b). At this instant the voltage between terminals 1–3 is equal to zero and assumes a sawtooth form between instants t_1, t_2, etc., the instantaneous amplitude of the sawtooth being equal to the difference between the instantaneous value of the function and its value at the time of last sampling. Since the intervals of time between samples are very short, the function can be assumed to be linear between these samples and the average value of the sawtooth is therefore $\frac{1}{2}[E(t_n) - E(t_{n-1})]$, which is nearly equal to $\frac{1}{2}(de/dt)$. The filter F in Fig. 8(a) does the averaging.

Integration and Differentiation with Respect to a Variable Other Than Time

Fig. 9(a) and 9(b) shows block diagrams whereby y can be integrated, or differentiated, with respect to x. The computer makes use of components which have been described above:

1) Integration $z = \int y dx$ [Fig. 9(a)]

Step 1—x is differentiated to dx/dt.
Step 2—y and dx/dt are multiplied to obtain ydx/dt.
Step 3—$y(dx/dt)$ is integrated with respect to time to obtain the desired result $\int ydx$.

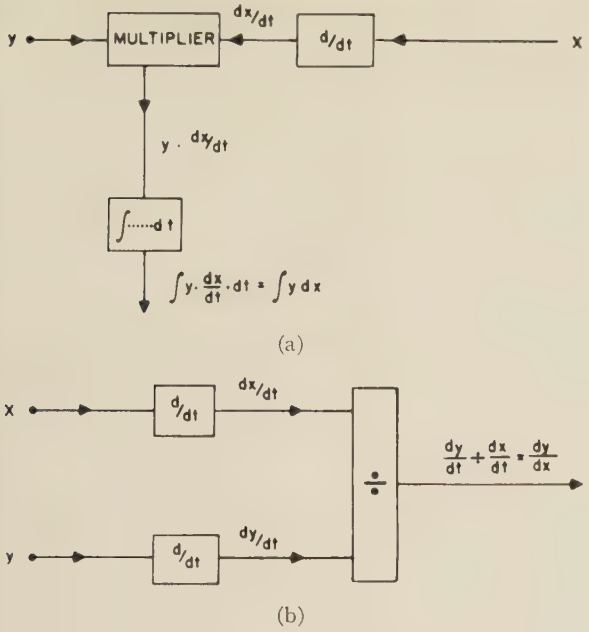


Fig. 9.

2) Differentiation $z=dy/dx$ [Fig. 9(b)]
Step 1—y is differentiated to dy/dt.
Step 2—x is differentiated to dx/dt.
Step 3—dy/dt is divided by dx/dt to give dy/dx, the desired derivative.

Other Applications

Many other applications of this sampling parametric method of calculation will suggest themselves. Thus it is possible

1) To determine sin $(nx+\theta)$ when sin x is known by generating the two waves and sampling one at the instant that the other reaches the known value.
2) To set up special series such as $z=Aa^x+Bb^{2x}+Cc^{nx}$ and to solve these series explicitly and implicitly.
3) To add voltages (E_y, E_x for example) relative to a common point and get an answer relative to this common point.
4) To multiply by a constant n.

Appendix I

A computer was constructed to test the theory outlined above and determine possible accuracy. This computer solves the equation

$$E_5 = E_3\left[\frac{E_1}{E_2}\right]^a - E_4\left[\frac{E_1}{E_2}\right]^b \tag{41}$$

where any of the voltages, or combination of voltages, may be treated as independent variables and the exponents a and b can be any real numbers.

Fig. 10 shows the manner in which the equation is related to the exponential discharge curves of the computer. Fig. 11 shows the block diagram of the computer which repeats its operation 60 times per second.

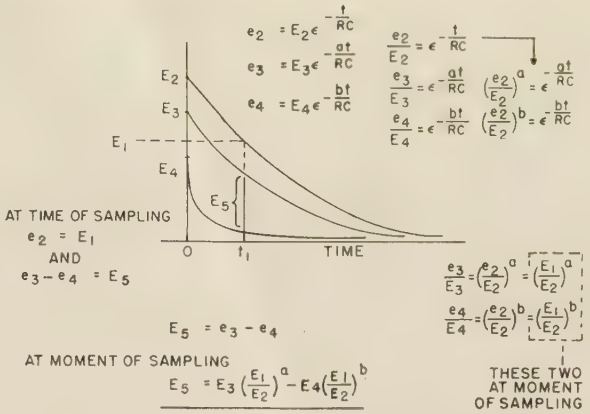


Fig. 10.

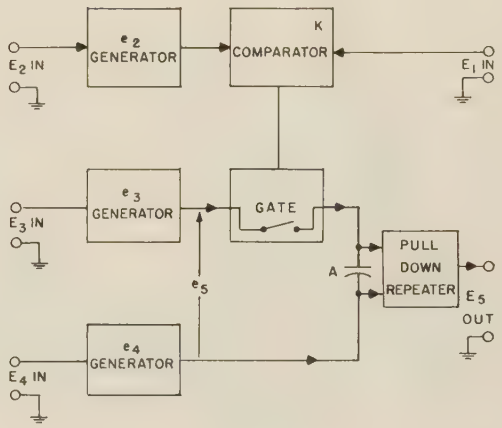


Fig. 11.

Three identical circuits are used to generate the exponential waveforms. The dc voltages E_2, E_3, and E_4 determine the starting voltage of the e_2, e_3, and e_4 exponential waveforms and each decay rate is determined by the RC time constant of its associated circuit. The exponents a and b are related to the time constants by:

$$a = \frac{R_2C_2}{R_3C_3} = \frac{\text{time constant of } e_2}{\text{time constant of } e_3} \tag{42}$$

$$b = \frac{R_2C_2}{R_4C_4} = \frac{\text{time constant of } e_2}{\text{time constant of } e_3}. \tag{43}$$

The several decaying voltages e_2, e_3, e_4, and e_5 are related to each other by the following equations

$$e_2 = E_2\epsilon^{-t/RC};\ \text{whence } e_2/E_2 = \epsilon^{-t/RC} \tag{44}$$

$$e_3 = E_3\epsilon^{-at/RC} = E_3[\epsilon^{-t/RC}]^a = E_3[e_2/E_2]^a \tag{45}$$

$$e_4 = E_4\epsilon^{-bt/RC} = E_4[\epsilon^{-t/RC}]^b = E_4[e_2/E_2]^b \tag{46}$$

$$e_5 = e_3 - e_4 = E_3[e_2/E_2]^a - E_4[e_2/E_2]^b. \tag{47}$$

At the time t_1, that e_2 voltage falls to the value equal to E_1, (Fig. 10) the comparator (Fig. 11) operates the diode switch which then charges the capacitor A to a value $(e_3-e_4)=E_5$ at that instant.

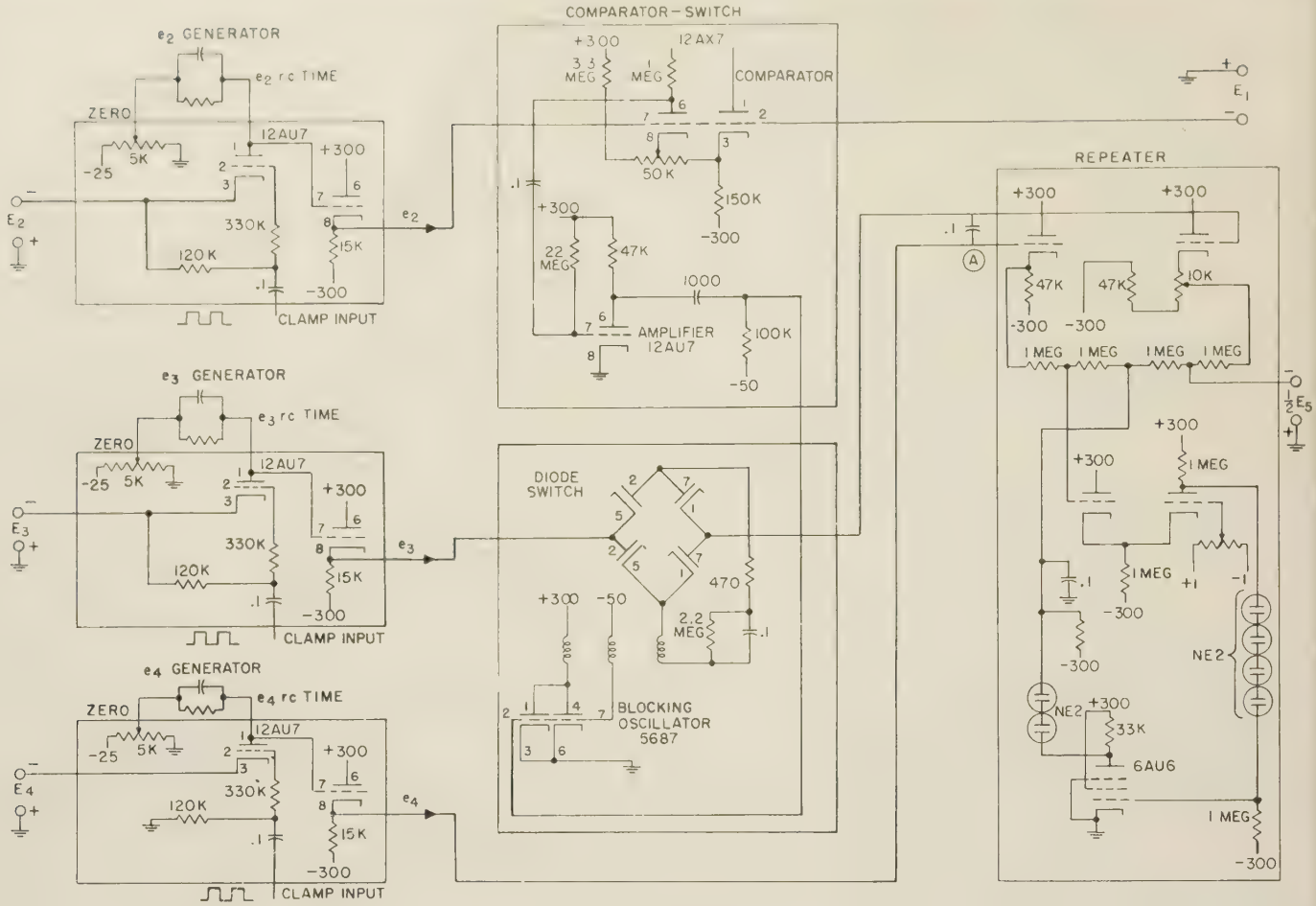


Fig. 12.

The repeater reproduces the dc voltage on capacitor A at the output terminals designated E_5. This voltage is

$$E_5 = (e_3 - e_4 \text{ at time } t_1) = E_3\left(\frac{E_1}{E_2}\right)^a - E_4\left(\frac{E_1}{E_2}\right)^b. \qquad (41)$$

Referring to Fig. 12, the clamp waveform, which is shown at the bottom of each generator, is supplied from a large 60-cycle sine wave which is amplified and limited to give a square wave. This sine wave determines the rate at which the computation is repeated.

During the positive half of the clamp wave, the circuit for the e_2RC time is clamped to the voltage E_2. Because of the clamp circuits chosen, the voltages E_1, E_2, E_3, E_4, and E_5 are all negative with respect to ground. When the negative half of the clamp wave occurs, the clamp tube stops conducting and RC circuit begins to rise toward zero at a rate determined by the RC time constant of the values chosen for the resistor and capacitor. The cathode follower provides a low-impedance output for the generator, but introduces a dc difference between its grid and cathode. In order that it be independently accurate in dc level, the stationary end of the RC circuit is returned to a point below ground so that when the RC circuit is fully discharged, the cathode follower gives zero dc volts output.

The output of the e_2 generator goes to the comparator, where it is compared with the dc voltage E_1. As the voltage e_2 becomes less negative, it finally reaches the value of E_1 volts, and causes plate current to flow in the 1-meg plate resistor of the comparator. The sudden negative swing of the plate is amplified through the 12AU7 amplifier and triggers the blocking oscillator.

The blocking oscillator causes conduction through the diode switch, and connects e_3 and e_4 to the capacitor A for a period of 10 microseconds. The dc voltage across A represents the answer, but both sides of the capacitor have a common potential which has both ac and dc components relative to ground.

The method used for repeating the dc voltage difference with one side grounded, is to reverse with respect to ground, and take the average of the voltage e_3 and $-e_4$ which is $\frac{1}{2}(e_3 - e_4)$ or $\frac{1}{2}E_5$. Both voltages e_3 and e_4 are repeated through cathode followers to avoid loading the charge on capacitor A. The voltage e_4 is reversed by using feedback across the two 1-megohm resistors at the left in Fig. 3. The midpoint of the two resistors is

kept at ground potential by applying to one end of the resistors a feedback signal which is equal and opposite to e_4. The two 1-megohm resistors to the right are used to obtain the average between e_3 and $-e_4$ which gives the desired output.

In operating the equipment, the value of E_1 must always be less than E_2, and the minimum value of E_1 that can be used is determined by the minimum value that e_2 reaches at the end of its exponential decay cycle. If the RC product is chosen equal to 0.2 of the available decay time, then values down to 0.006 of full scale are possible.

The accuracy obtained with the present equipment is between 1 and 2 divisions over most of the meter scale of 100 divisions, except at the end of scale above 95 where some problems produce errors of 4 divisions.

By reconnecting the elements of the computer as shown in Fig. 13, the output obtained is the time integral of the input voltage. The potentiometer is normally set near the top of its range. If E_1 is zero, the comparator will close the switch when the supply voltage reaches the voltage e_c, thus maintaining whatever charge is in C.

If the voltage E_1 is greater than zero, the switch will close at the time that the supply voltage reaches E_1 volts above e_c. Thus e_c+E_1 volts are placed across C. Because the change that occurs in e_c is always equal to E_1, it follows that e_c is the integral of E_1 for the number of samples taken, or if the repetition frequency is constant, for the amount of time elasped.

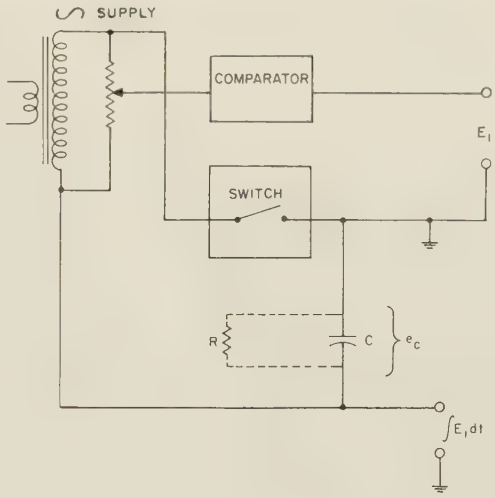


Fig. 13.

Because some leakage, R, exists, the supply to the switch is made greater than the supply to the sample, and thus keeps the charge from draining off from C.

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[2] United States Patent Number 2,652,194, September, 1953.
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[4] United States Patent Number 2,671,608, March 9, 1954.

Correspondence

A Gray Code Counter*

A binary counter may be programmed to count according to the reflected (Gray) code.[1] A suitable block diagram for four stages is shown in Fig. 1. The counts are fed into flip-flop F_0 whose two differentiated outputs are utilized to trigger the counter proper consisting of F_1, F_2, F_3, and F_4.

Each flip-flop consists of two tubes, one of them conducting at a time, and the following conventions will be followed throughout this discussion in describing their states. A tube at cutoff represents a zero, and a conducting tube a one; in flip-flop F_0, a trigger will be generated by the tube which is changing from zero to one; finally, it will be assumed that the lower half of F_1, F_2, F_3, and F_4 represents the binary number contained in the counter. In our case, this number is 0110 which corresponds to 4, in the reflected code.

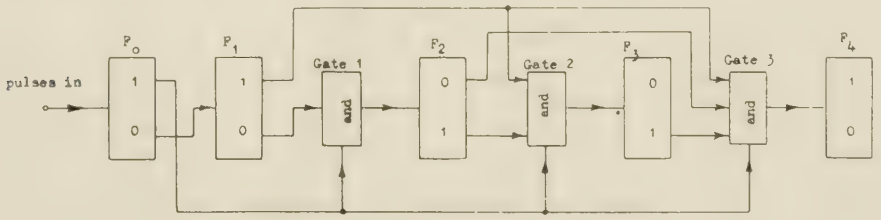

Fig. 1.

The operation of the counter will now be described. One trigger produced by F_0 is connected directly to F_1, and the other one to a bus bar feeding all the other counter stages through "and" gates. The proper gating action is provided by the flip-flops F_1, F_2, and F_3. The "and" gates will transmit the trigger from F_0 only if all their other inputs are "one." In Fig. 1, the next trigger from F_0 will flip F_1, consequently changing the state of the counter to 1110. This corresponds to 5. The next trigger from F_0 is transmitted to all gates. However, only gate 1 is open, and, consequently, F_2 is triggered. The count is now 1010, corresponding to 6. Fig. 2 shows a practical diagram of a reflected code binary counter containing six stages.

Throughout a regular counting sequence, the trigger will appear alternatively at the input of F_1, or at the bus leading to all gates. The counting direction will be reversed by a single repetition of the trigger at that point where it appeared last. For instance, starting with 1010, corresponding to 6, the last trigger appeared at the bus leading to all gates. Another trigger applied to the same point will find gate 1 still open, and return F_2 to its previous state 1. The count is now 1110, corresponding to 5. The next regular count flips F_1 and produces 0110, corresponding to 4.

This reversing property of the counter enables one to build a forward backward counter, and Fig. 3 shows the logical arrangement for the input stage of such a counter. A separate input is provided for additive and subtractive counts. In the state shown, an input pulse at the "add" terminal first flops F_0. Then it produces, after the delay necessary for F_0 to reach the steady state, an output at the gate bus. A subsequent pulse at the "subtract" terminal returns F_0 to its previous state and again produces an output at the gate bus, as required.

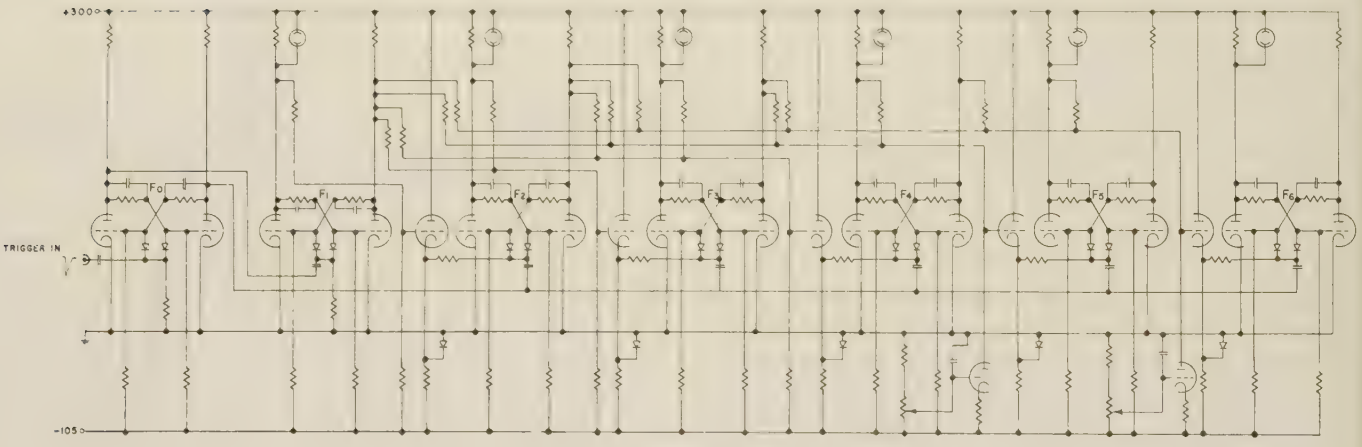

Fig. 2.

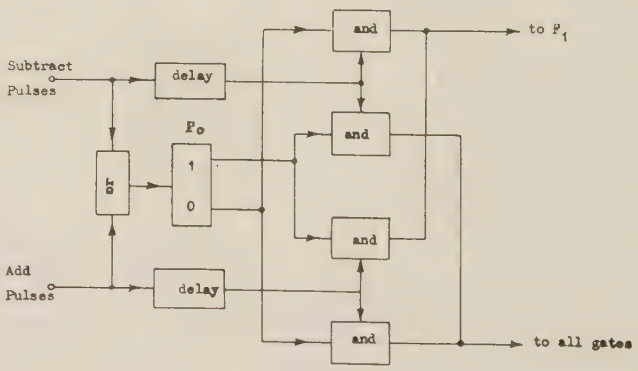

Fig. 3.

* Received by the PGEC, December 14, 1956.

[1] F. A. Foss, "The use of a reflected code in digital control systems," IRE TRANS., vol. EC-3, pp. 1–6; December, 1954.

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A Method for Obtaining Complete Digital Coding Chains*

Given K different symbols (*e.g.*, the digits 0, 1, 2, $\cdots$, $K-1$), one can always write a closed loop in which each symbol appears K^{n-1} times, arranging the symbols in such order that every subsequence of n contiguous symbols is unique. It is then possible to read K^n different code combinations or numbers, corresponding to the K^n different reading stations for the set of n symbols. This assertion can be proved by showing that the permutation scheme described below is exhaustive. A forthcoming SCEL report[1] will contain such proof.

Johnson[2] has described sequences of this kind for binary digits. He calls them "binary chains" and attributes their discovery to Baudot. Johnson shows methods which assist in the discovery of "complete" binary chains, (*i.e.*, sequences which contain all 2^n n-bit combinations), but his rules do not work predictably in all cases. By contrast, a method in use at SCEL gives complete chains for any radix and any n. This method is as follows:

1) Assign to K symbols an arbitrary "order of preference."

2) Imagine a "register" consisting of n boxes. Fill this register with the *last preferred symbol* written n times.

3) Shift the contents of the register one place in either direction. One symbol will overflow out of the register and a box will become vacant at the opposite end. Write the *first preferred symbol* in the vacant box.

4) Continue to shift the contents of the register in the same direction. Continue to write the first preferred symbol in the vacant box after every one-place shift; then compare the new combination of symbols in the register with all previous combinations. Eventually, a combination will repeat. When this occurs, remove the first preferred symbol just written and replace it with the second preferred symbol. If the second preferred symbol also gives a repeat, use the third, etc., but do not violate the order of preference.

The above process gives all possible permutations of the symbols before it is exhausted. It follows that the sequence of symbols occupying any one box forms a complete coding chain when closed upon itself.

For example, let K be three, let 0, 1, and 2 be the three symbols in order of preference, and let n be two. Shifting the register contents to the left, we get in succession:

22
20
00
01
10
02
21
11
12.

In the endless chain made by closing 220010211 on itself, all nine two-place ternary numbers can be obtained by reading two adjacent digits.

For binary chains, one may start with all 0's and try 1's first. For large n, it is convenient to consider the successive n-digit combinations as conventional binary numbers in order to use their decimal equivalents as a shorthand for generating the sequences.

The rule for left-hand shift is, then, to start with zero and to perform repeatedly the following process:

Double modulo 2^n, and add unity to make an odd number. If the resulting odd number is a repeat, subtract unity from it, to make it even. Either the odd number or the even will be new, until both unity and zero repeat after 2^n different numbers. Thus, giving n the value four, we get 0, 1, 3, 7, 15, 14, 13, 11, 6, 12, 9, 2, 5, 10, 4, 8. By writing an 0 for every even number and a 1 for every odd, we get 0111101100101000 which is a complete binary chain of 16 places.

In general, the process described defines $2K!$ different chains for all K and all $n \geqq 2$, corresponding to all possible orders of preference for K symbols and to both directions of shift. (Known exceptions are $n=2$ or 3 when $K=2$, for which unique chains occur.) Nevertheless, there are other complete chains not obtainable in this way.[3] Thus, neither 1111010000101100 nor 221001120 is obtainable by these rules.

In general, the binary chains described herein do not coincide with those of Johnson.

Neither Johnson nor the authors have yet found a simple means of translating to conventional number codes.

One possible use for chain codes is in inventory or catalog systems employing cyclicly interrogated digital memories such as magnetic drums. With a complete binary chain, only 2^n bits are needed to record 2^n catalog numbers or addresses, while still recording the entire address for every location —a possible saving of $(n-1)2^n$ bits.

Here, the difficulty of translating to natural numbers is no handicap. Other applications can be visualized in data transmission, in certain special analog-to-digital conversions, and in some digital data processing. Where "incomplete" chains can be devised with superior capability for translation, etc., they may be preferable in all the latter cases.

Acknowledgment

The permutation process outlined above evolved from a suggestion by Leon Goroff of the Signal Corps Engineering Laboratories. Jacob Borsuk and Jerome Rothstein of SCEL and Jack Breckman of the Radio Corporation of America contributed to the study of the codes and to mathematical proof of the permutation process. Jack E. Volder of Convair first brought the complete chains problem to the attention of one of the authors.

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* Received by the PGEC, February 15, 1957.

[1] B. Lippel and I. J. Epstein, "Methods for Obtaining Complete Digital Coding Chains," Signal Corps Eng. Labs. Tech., Memo. M-1850; June, 1957.

[2] E. A. Johnson, "A Chain Code of Binary Symbols," Radar Res. Establishment Tech. Note No. 359, Ministry of Supply, Malvern, Worcester, Eng. (ASTIA Reference: AD #65071); January, 1957.

[3] As this note goes to press, a new reference has come to our attention in which De Bruijn computes the total number of complete binary chains to be 2^{m-n}, where $m=2^{n-1}$.

N. G. De Bruijn, "A combinatorial problem," *Proc. Nederl. Acad. Wetensch.*, vol. 49, pp. 758–764; 1946.

A Survey of the Characteristics of Currently Used Bistable Multivibrators*

A survey of the characteristics of currently used bistable multivibrators has recently been carried out in the College of Engineering at the University of Wisconsin, with the aim of collecting a body of data and comparisons which might assist those faced with the selection or design of such circuits.

The analysis of a bistable multivibrator or even the synthesis of this circuit in accordance with dc or steady-state considerations is a relatively simple matter. The transient analysis, however, which endeavors to determine the resolving time or maximum repetition rate, is much more involved. For ease of discussion, the resolving time may be separated into: 1) the settling time, which is dependent on various RC time constants and is a measure of the time which must elapse from the completion of flip-flop transition until the circuit can be successfully triggered again, and 2) the transition time which involves all the circuit elements including the tube characteristics and their associated nonlinear effects. The transition time is particularly difficult to calculate accurately, and in most cases is a byproduct of the dc circuit design.

In an effort to overcome these difficulties, an attempt has been made to determine experimentally various circuit characteristics by compiling data on a number of flip-flop circuits which have been used commercially in sizeable quantities by various manufacturers and universities. A standard questionaire was sent to 143 organizations in the United States, Canada, and England. In response to this, 88 replies were received, 58 of which comprised useful data. From over 75 circuits, 31 circuits were picked as representative, or chosen to be tested for purposes of comparison.

Whereas it is probably true that no two flip-flop applications can be satisfied by the same optimum circuit, it is hoped that the circuits included in this report will be diverse enough to satisfy specifications approximating those desired. Modifications made to these circuits in accordance with well-known theory should produce a satisfactory circuit with a minimum of effort.

A report describing the results of the survey has been published by the Engineering Experiment Station of the College of Engineering, University of Wisconsin. Requests for single copies of this report may be sent to the undersigned.

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* Received by the PGEC, February 19, 1957.

Unit-Distance Binary-Decimal Code Translators*

In a recent discussion of unit-distance binary-decimal codes,[1] Tompkins remarked that codes with simpler rules for translation to conventional constant weight codes might be found. Gilbert has enumerated all classes of unit-distance 4-bit binary-decimal codes.[2] From these it can be shown that there is only one distinct class of unit-distance 4-bit binary-decimal codes for two-track commutation in analog-to-digital converters. No unit-distance binary decimal code using four brushes in one track may be devised.[3] At least one unit-distance code using five brushes in one track is possible.[3,4]

First, consider a unit-distance code used on a particular angular position encoder and its associated translator which produces a desired output code. Permutation of this code corresponds to relabeling the brushes of the encoder in a different order or shifting the positions of tracks of each decimal digit radially, among themselves, without changing the labels on individual brushes. Appropriate relabeling of translator leads leaves its elements unchanged. Complementation of a code corresponds to interchanging conducting and nonconducting segments of selected tracks. This does not change the required total number of elements in the translator. All codes which may be generated by permuting and/or complementing a given code have translators of identical complexity and will be considered to be a single class of codes. Only the number of different classes of codes need be determined. One member of each class of code is then investigated in detail, to determine the number of translator elements for all codes of that class.

It should be noted that horizontal or vertical translation, rotation, reflection about a horizontal or vertical centerline or a left or right diagonal produces a map of a new code which in the same class as the original code and does not have an essentially different translator. Also, reflections about minor axes between the first and second square and between the third and fourth squares in either the vertical or horizontal direction do not produce a code of a new class. Some simple algebraic transformations of a code, such as permuting a and d, produce complex geometric changes in the occupied squares of a map.

In Tompkins' Fig. 2, the first and third maps in the left column are not related to each other by a single translation or a single rotation as are the other maps of the figure. Using McCluskey's method for detecting symmetry,[5] it can be shown that these codes are related by:

$$a_0 = c_3$$

$$b_0 = b_3$$

$$c_0 = a_3$$

$$d_0 = d_3'.$$

Using either of these maps, but not both, decimal zero may be placed in any of the 10 squares containing an x and the sequence may proceed in either direction. Evaluating the 20 different translators completes the analysis. Placing decimal zero in the upper left hand corner of the map and decimal 1 to the right of it permits the code words for 0, 1, 2, 3, 8, and 9 to differ only slightly from their usual binary values. That is, the encoder map fits the map of the translator output code well in a number of places.

Fig. 1, presented below, shows maps of two of the twenty maps using two different sets of coordinate labels.

The figure also shows values to illustrate the relationship of these maps to Tompkins' maps. However, this is not a rigorous proof that these choices require a simpler translator than the other 18 possibilities.

The logical expressions for translation to 1, 2, 4, 8 output code are given for both conventional numbering (requiring logical detenting) and for reflected decimal numbering notation.

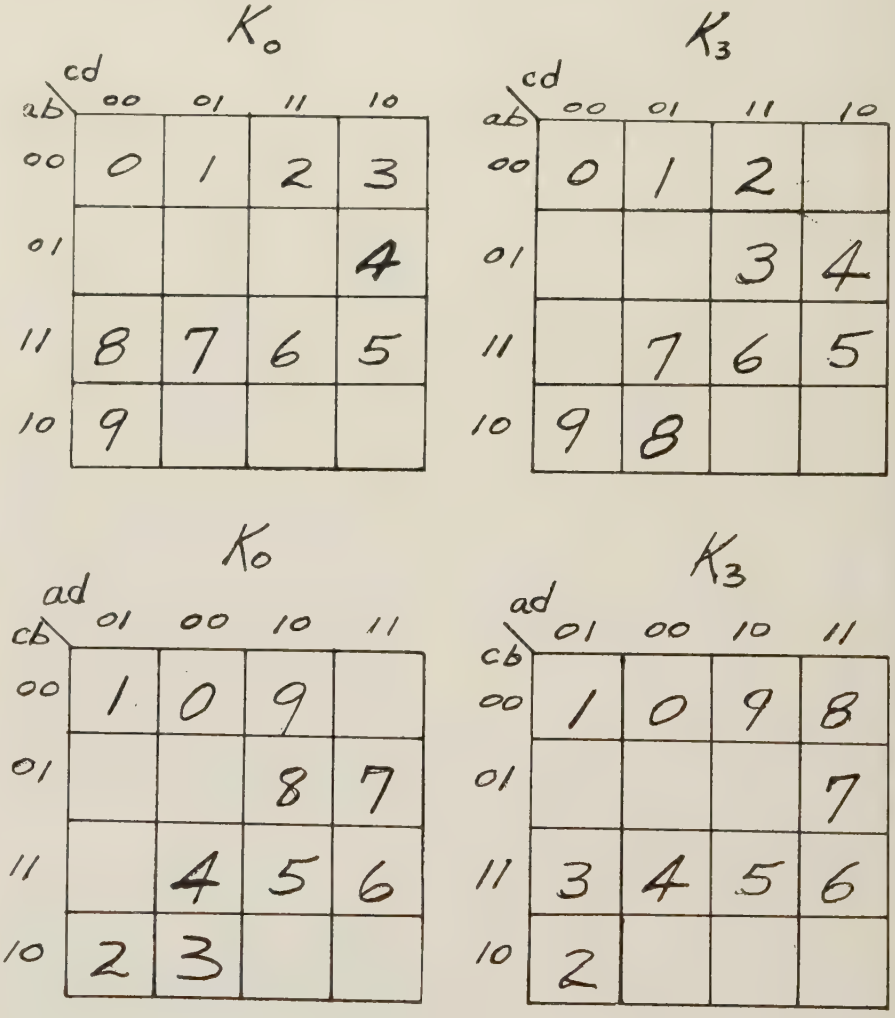

Fig. 1.

Logical Expression for Encoder Translators

a, b, c, d = Inputs from encoder brushes

1, 2, 4, 8 = Outputs from translator

e = 1 output from translator for next most significant decimal digit

K_0—Logical Detenting

$8 = ac'd'$ $\quad 2 = ad + b'c$

$4 = b(c + d)$ $\quad 1 = ab' + (a + b)(c'd + cd')$

K_0—Reflected Numbering

$8 = (ad'e' + a'b'e)c'$

$4 = b(c + d)e' + (a' + d')ce$

$2 = ad + b'c$

$1 = [ab' + (a + b')(c'd + cd')]e'$
$\quad + [a'b + (a'b)(c'd' + cd)]e$

K_3—Logical Detenting

$8 = ab'$ $\quad 2 = (b + c)d$

$4 = ab + cd'$ $\quad 1 = ad' + [a'b + (a' + b)c']d$

K_3—Reflected Numbering

$8 = ab'e' + a'c'e$

$4 = (ab + cd')e' + (a' + d')ce$

$2 = (b + c)d$

$1 = [ad' + [a'b + (a' + b)c']d]e'$
$\quad + [a'd' + b'c + ad(b' + c)]e$

* Received by the PGEC, February 20, 1957; revised manuscript received, March 14, 1957.

[1] H. E. Tompkins, "Unit-distance binary-decimal codes for two-track commutation," IRE Trans., vol. EC-5, p. 139; September, 1956.

[2] Unpublished.

[3] J. A. O'Brien, "Shift Register Decimal Counter," CP57-338. AIEE Winter General Meeting, Figs. 6a, 6b, 7a; January 25, 1957.

[4] W. H. Libaw and L. J. Craig, "A photoelectric decimal-coded shaft digitizer," IRE Trans., vol. EC-2, pp. 1–4; September, 1954.

[5] E. J. McCluskey, Jr., "Detection of group invariance or total symmetry of a Boolean function," *Bell Sys. Tech. J.*, vol. 35, pp. 1445–53; November, 1956.

Translators for either of the above reflected numbering schemes are more complex than translators for 4-bit reflected binary-decimal codes.[6] Two classes of codes permit conversion from reflected to conventional decimal number notation by complementing the output of one of four brushes in separate tracks where all pairs of words read from adjacent sectors are unit distance. The expression given in Tompkins' paper may be used with logical detenting between decades, but not reflected numbering. Glixon[7] has described a procedure using conventional numbering notation, where each decimal digit is assigned one of a pair of words (which differ in one bit) depending on whether the next more significant digit of a complete number is even or odd. Using this procedure with the unit-distance two-track code K, Tompkins' translator expressions apply. Indeed, Glixon's procedure extends the number of unit-distance codes that should be investigated for translator complexity because any unit-distance sequence of length ten may be used whether it closes or not.

ACKNOWLEDGMENT

The writer wishes to acknowledge the helpful comments of E. J. McCluskey and E. N. Gilbert.

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[6] J. A. O'Brien, "Cyclic decimal codes for analog-to-digital converters," *Trans. AIEE, Commun. and Electronics*, vol. 75, pp. 120–122; May, 1956.
[7] H. R. Glixon, "Can you take advantage of the cyclic binary code?," *Control Eng.*, vol. 4, pp. 87–91; March, 1957.

Negative Base Number Systems*

It is commonly stated that any positive integer r greater than unity can be used as the base of a number system. Thus, a number is expressed by a polarity sign (plus or minus) together with a shorthand notation for $(a_n r^n + a_{n-1} r^{n-1} + \cdots + a_1 r + a_0 + a_{-1} r^{-1} \cdots)$, viz, $\pm a_n a_{n-1} \cdots a_1 a_0 \cdot a_{-1} \cdots$, the base being previously agreed upon, and the a_i are integers $0 \leq a_i < r$. However, it appears that negative integers may also be used as bases. For example, 101101 would represent in a "negative two" system the decimal equivalent -35, derived from $(-2)^5 + 0 \cdot (-2)^4 + (-2)^3 + (-2)^2 + 0 \cdot (-2) + 1 = -32 + 0 - 8 + 4 + 0 + 1 = -35$. Similarly, 10011 represents $+15$, and 1.11 represents $+0.75$. Notice that in a "negative base" system a separate sign indication is not required, the sign being self-contained. Table I of "negative two" equivalents follows.

It will be noted that any positive or negative number can be represented. Whether a number in this notation is positive or negative can be found by inspection, positive integers having an odd number of figures, negative integers an even number of figures.

TABLE I

Negative	Number	Positive
0	zero	0
11	one	1
10	two	110
1101	three	111
1100	four	100
1111	five	101
1110	six	11010
1001	seven	11011
1000	eight	11000
1011	nine	11001
1010	ten	11110
110101	eleven	11111
110100	twelve	11100
110111	thirteen	11101
110010	fourteen	10010
110101	fifteen	10011
110000	sixteen	10000

The necessary addition and multiplication tables are given below.

Addition

	0	1
0	0	1
1	1	110

Multiplication

	0	1
0	0	0
1	0	1

[Subtraction rules can be inferred from the above, but a straightforward procedure is simply to multiply by minus one (*i.e.*, 11) and add.]

Note the "double carry" that is required in adding 1 to 1. In many cases of practical addition or multiplication, this results in a nonending sequence of carries to the left; but once the carry passes out of field, the remaining representation is correct. For example, adding minus one to minus one:

$$\begin{array}{r} 11 \\ +\ 11 \\ \hline \cdots 111 \\ \cdots 111 \\ \cdots 00010 \end{array} \quad \begin{array}{l} \\ \\ \left.\begin{array}{l}\\ \\ \end{array}\right\}\text{carries} \\ \text{sum} \end{array}$$

No attempt is made to assess the practical value of a "negative base" system. However, its advantage of a set of rules for arithmetic free from dependence upon a prefixed polarity sign appears worth examining.

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A Fast Circulating Memory*

The recent development of diffused base transistors with alpha cutoff frequencies above 200 megacycles makes it possible to build very fast logical circuits. By making use of some of these circuits in the regeneration logic of a circulating memory, a very short access time can be realized. One application of such a fast small capacity memory might be to replace many of the registers of a parallel computer. To do this, a number of delay lines equal to the number of digits in the computer word would be used and would be circulated in synchronism by a common clock signal. The number of digits in any one delay line would be equal to the number of registers required.

As an illustration of the speeds attainable a small memory was built using an ordinary coaxial cable as the delay line and experimental Western Electric transistors in the regeneration logic. Eight digits were stored in the line and were circulated by means of the regeneration logic shown in Fig. 1. The regeneration is accomplished by

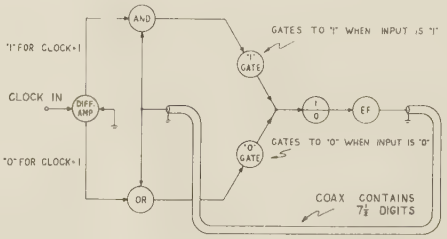

Fig. 1—Logical diagram of delay line memory.

using a flip-flop, at the input to the cable, which is set on each clock cycle to agree with the state of the output end of the cable. The timing of the various points of the circuit is shown in Fig. 2, which is drawn to represent

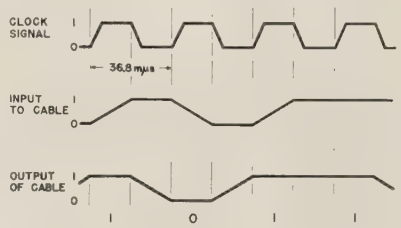

Fig. 2—Timing diagram.

the circuit operation near the maximum speed so that a clock period is equal to twice the time required to change the state of the flip-flop. Note that a nonreturn-to-zero system is used which permits the storage of a larger number of digits in the same length of cable. With the choice of clock period above, the output end of the cable remains in the same state throughout the length of the flip-flop gate signal ($\frac{1}{2}$ clock cycle). This is required for the maximum speed of gating. The length of the cable is chosen so that the delay is $7\frac{1}{2}$ clock cycles; the other $\frac{1}{2}$ cycle is the time required to set the flip-flop.

For the test circuit the cable was 212 feet of RG62/U cable which has a delay of 276 mμs. For this delay to contain $7\frac{1}{2}$ clock cycles, the clock frequency was made equal to 27.2 megacycles. The transistors were Western Electric type GA-53233 diffused-base *p-n-p*. The memory so produced stored eight digits with a maximum access time of 295 mμs. Since the cable delay is only about 1.3 mμs per foot, the exact length of the cable for a given clock frequency is not critical. An error of a foot or two in the above cable probably would not be noticeable in the circuit performance.

Fig. 3 is a circuit diagram of the test

* Received by the PGEC, February 23, 1957.

* Received by the PGEC, March 14, 1957.

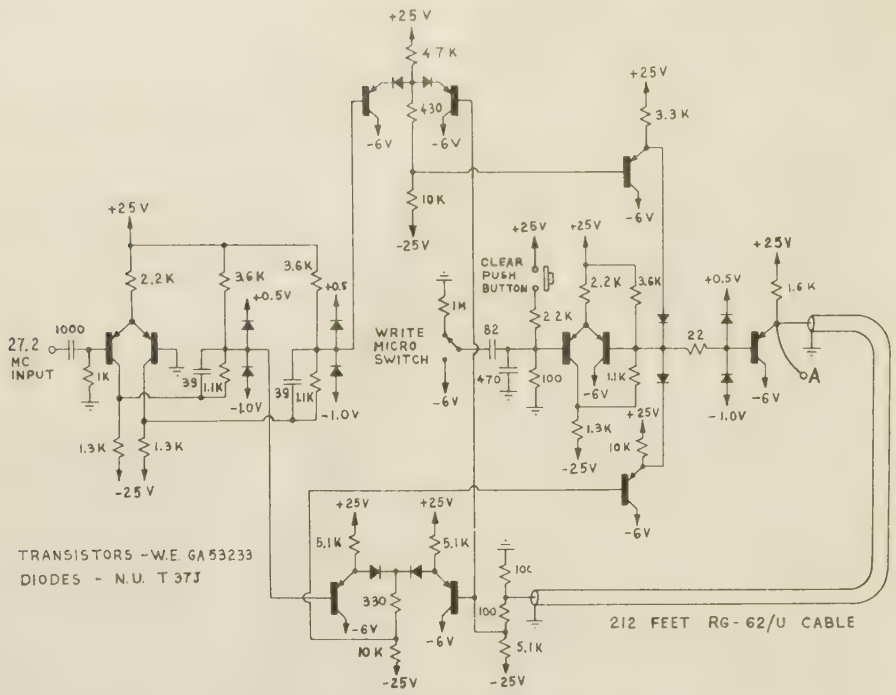

Fig. 3—Circuit diagram of test memory.

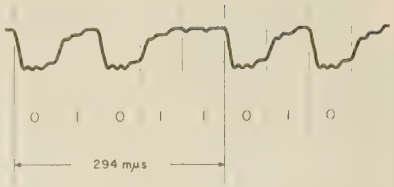

Fig. 4—Typical waveform in delay cable.

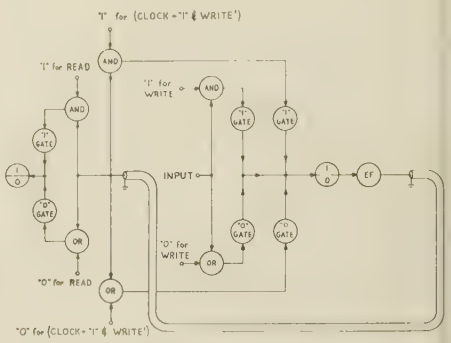

Fig. 5—Memory with READ and WRITE logic.

memory. Two transistors are required to generate a push-pull clock signal. In a large-scale memory this part of the circuit would be constructed only once for the whole memory. The rest of the circuit would be required for each cable used in the memory. The write-in circuit which was used in this test memory was made as simple as possible to minimize the number of transistors required. It therefore merely sets the flip-flop at some random time and is used only to produce typical storage patterns.

A typical waveform at the input end of the cable, point A of Fig. 3, is shown in Fig. 4. The clock frequency is only 17 mc and there are only five digits stored in this figure, but the waveform is typical for the operation near the upper limit of speed. It has the same shape as did the same signal at 27.2 mc originally. The lower frequency of operation was necessary, because one of the original transistors drifted in its characteristics so as to be unusable before this waveform was recorded and a replacement was not available because of a shortage of these transistors. When a transistor of lower alpha than the actual design limit of the circuits was substituted, the maximum speed of operation was reduced.

In order to get information into and out of an actual memory, some additional logic is required. The logical diagram of one way to do this is shown in Fig. 5. The READ and WRITE signals coincide with the particular clock pulses to affect the position desired in the cable. The techniques for generating these signals could be the same as are already in wide use in serial computers.

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Contributors

Hiroshi Amemiya (S'52–A'53) was born in Tokyo, Japan, on March 3, 1927. He attended the University of Tokyo and received the degree of Bachelor of Engineering (Kogakushi) in electrical engineering in 1948. From 1948 to 1949, he was employed by the Japan Victor Co., where he was concerned with the production of loudspeakers.

In 1950 he returned to the University of Tokyo for further study in electrical communications engineering. He came to the United States in 1952 to participate in the International Educational Exchange Program of the U. S. Government. During his stay in the United States, he studied at Cornell University and received the M.S. degree in 1954. He joined Showa Denshi, Ltd., in 1956.

Mr. Amemiya is a member of the Institute of Electrical Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, and Sigma Xi.

❖

Gene W. Arant was born in North Powder, Ore., on December 21, 1920. Receiving the B.S. degree in electrical engineering from Oregon State College in 1943, he then entered the U. S. Army and attended the radar course at Harvard University and the Massachusetts Institute of Technology. For two years thereafter, he was a technical liaison officer at the National Bureau of Standards.

In 1946, Mr. Arant studied law at the University of Southern California, where he also served as a teaching assistant in electrical engineering prior to receiving the L.L.B. degree in 1949. After a brief period of private law practice in Los Angeles, he was recalled to military duty and became a contracting officer at the Army Guided Missile Center, Huntsville, Ala.

Mr. Arant then entered the employ of Hughes Aircraft Company and subsequently The Ramo-Wooldridge Corporation, specializing in the patenting of electronic computer developments. He is now practicing patent law in Long Beach, Calif.

Mr. Arant is a member of Tau Beta Pi, Eta Kappa Nu, and Pi Mu Epsilon.

❖

Elmer G. Gilbert (S'51–A'52) was born on March 29, 1930, in Joliet, Ill., He received the B.S.E. degree in electrical engi-

neering in 1952, the M.S.E. degree in electrical engineering in 1953, and the Ph.D. degree in instrumentation engineering in 1957, all from the University of Michigan.

Since 1953, Dr. Gilbert has been an Instructor in the Department of Aeronautical Engineering at the University of Michigan. His activities there include work in automatic control, electronic analog computation, and flight simulation.

He is a member of Eta Kappa Nu, Phi Kappa Phi, Tau Beta Pi, and Sigma Xi.

❖

Fred C. Hallden (SM'54) was born in New York, N. Y., on September 8, 1919. He received the B.S. degree in Physics in 1953 from Hofstra College. From 1941 to 1943, he was with International Business Machines Corp. as a service engineer, and then spent a year with Standard Electronics Research Corp. and a year with Mechtronics Corp.

Since 1945, he has been with the Hazeltine companies in Little Neck, N. Y., and during these years he has worked on radar (aew), identification (iff), and subminiaturization in connection with various military contracts. His work at present is largely devoted to research and development on transistor circuits and analog computer circuits.

❖

Bernard Harris (S'48–A'52) was born on October 13, 1927, in New York, N. Y. He received the B.E.E. degree from Cooper Union in 1949, the M.S. degree from Columbia University in 1951, and is currently studying for the D.Eng.Sc. degree at Columbia University.

From 1946 through 1947, he served in the U. S. Army as a radio instructor. From 1949 through 1951, he was a graduate assistant in the Electrical Engineering Department at Columbia University. From 1951 to 1954, he was employed at the New York Industry Service Laboratory, RCA Laboratory Division, as a television development engineer concerned with the design of uhf tuners and the application of transistors to broadcast band radio and television receivers.

Since 1954, Mr. Harris has been engaged in communication and information theory applications at the Research Division of New York University.

He is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi.

❖

Charles J. Hirsch (M'39–SM'43–F'51) was born in Pittsburgh, Pa., on October 25, 1902. He received the A.B. and E.E. degrees from Columbia University in 1923 and 1925, respectively. He spent some time in the radio engineering departments of F. A. D. Andrea, Thomas A. Edison, Inc., and John Hays Hammond Laboratories until 1933, and from 1933 to 1937 he worked in France and Italy as chief engineer in radio companies there. From 1937 to 1942, he was chief engineer of Majestic Radio Corp. in Chicago. He joined the Hazeltine companies in 1942 and is now Executive Vice-President of Hazeltine Research Corporation.

During his years in the electronic industry, Mr. Hirsch has been especially active in the fields of radio aids to navigation, computers, radar, and iff systems, and lately has spent a great deal of time on color television. For his work during World War II in design and development of radar and iff systems, he was awarded the U. S. Navy Certificate of Commendation in 1947. He was secretary of Panel 13 (Color Video Standards) of the NTSC, the industry organization which developed the specifications for color television standards in the U. S. Since 1955, he has been chairman of the United States Preparatory Committee for CCIR Study Group XI, which concerns itself with television, particularly color television standards for Europe, and in 1956 was chairman of the United States delegation to color television demonstrations in the United States, France, England, and the Netherlands.

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Robert M. Howe, for biography see page 256 of the December, 1956, issue of these TRANSACTIONS.

❖

David C. Kalbfell (A'44–SM'45) was born in Indianapolis, Ind., on August 20, 1914. He received the A.B. degree from U.C.L.A. in 1934.

Mr. Kalbfell received his doctorate in nuclear physics from the University of California in 1939, but most of his professional career has been in the field of electronics. He worked for the Standard Oil Company of California for two years, and the Office of Scientific Research and Development for five years during the war. He then founded Kalbfell Laboratories (later changed to Kay Lab and Kin-tel). He taught part time at the University of California from 1943 to 1948, and at San Diego State College from 1948 to 1956.

He is now a consultant for Beckman Instruments, Lockheed Missile Division, and Ampex Corp. and owns Kalbfell Electronix, a research company.

Dr. Kalbfell is a member of Phi Beta Kappa, Sigma Xi, Pi Mu Epsilon, AIEE, and ACM.

❖

Mitchell P. Marcus was born in Boston, Mass., on January 5, 1922. He received the B.I.E. degree from Ohio State University in 1948. Since that time, he has been associated with the International Business Machines Corporation.

He is currently a member of the Engineering Planning Department in the Endicott Product Development Laboratory, where his work is primarily concerned with switching circuits, systems, and logical design. He also teaches courses in switching circuit logic and design, and arithmetic systems and devices to IBM engineers. Mr. Marcus is a member of Tau Beta Pi.

❖

Toshio Numakura was born in Tokyo, Japan, on September 26, 1929. He graduated from Tokyo Institute of Technology with the B.S. degree (Kogakushi). In 1953, he joined Central Research Laboratory, Hitachi, Ltd., where he has since been primarily engaged in the development, design, and application of electronic analog computers.

He is a member of the Institute of Electrical Engineers of Japan.

❖

Amos Nathan (S'50–A'51–M'55) was born in Liegnitz, Germany, on October 5, 1920. He entered Palestine in 1933 and received the degree of Dipl. El. Mech. Engineer from Technion, Israel Institute of Technology, Haifa, Israel, in 1943.

He served with the British Forces from 1942 to 1946. From 1946 to 1948, he was an assistant at Technion. He then served in the Israel Defence Force until 1953, attaining the rank of major. After a year of study in the United States, he received the M.S. degree in electrical engineering from Columbia University in 1951. In 1956, he received the degree of doctor of science from Technion.

Dr. Nathan rejoined the staff of Technion in 1953, where he is now a senior lecturer in electrical engineering, and he also has charge of an electronic differential analyzer project.

Dr. Nathan is an associate member of IEE, London.

❖

Takeo Miura was born in Kyoto, Japan, on October 1, 1925. He graduated from Kyoto University, Japan, with the B.S. degree (Kogakushi). He joined Hitachi, Ltd., in 1949 and was engaged in the design of induction motors at Kameido Works. In 1950, he was transferred to Central Research Laboratory, where he has since been engaged in the development of electronic analog computers, regulators, and servomechanisms.

Mr. Miura is a member of the Institute of Electrical Engineers of Japan.

PGEC News

1957 WESCON

The 1957 Western Electronic Show and Convention will be held in San Francisco for the four days of August 20–23. The deadline for papers has passed. Inquiries about the meeting may be directed to the business office, 342 North La Brea, Los Angeles 36, Calif.

Distribution of PGEC Members; Paid Membership by Sections as of December 31, 1956

Sections	*No. of Members*
Akron	29
Alamogordo-Holloman	11
Albuquerque-Los Alamos	26
Atlanta	39
Baltimore	114
Bay of Quinte	4
Beaumont-Port Arthur	2
Binghamton	61
Boston	448
Buenos Aires	2
Buffalo-Niagara	26
Cedar Rapids	19
Central Florida	42
Chicago	160
China Lake	10
Cincinnati	33
Cleveland	35
Columbus	13
Connecticut Valley	118
Dallas	31
Dayton	40
Denver	19
Detroit	120
Egypt	0
Elmira-Corning	4
El Paso	18
Emporium	19
Evansville-Owensboro	6
Florida West Coast	1
Ft. Huachuca	1
Ft. Wayne	16
Ft. Worth	27
Hamilton	4
Hawaii	1
Houston	44
Huntsville	30
Indianapolis	22
Israel	10
Ithaca	22
Kansas City	24
Little Rock	9
London	4
Long Island	269
Los Angeles	715
Louisville	8
Lubbock	6
Miami	12
Milwaukee	49
Montreal	38
Newfoundland	2
New Orleans	13
New York	618
Northern Alberta	3
Northern New Jersey	252
Northwest Florida	7
North Carolina-Virginia	33
Oklahoma City	9
Omaha-Lincoln	5
Ottawa	14
Philadelphia	447
Phoenix	10
Pittsburgh	52
Portland	14
Princeton	29
Regina	1
Rio de Janeiro	1
Rochester	25
Rome-Utica	37
Sacramento	7
St. Louis	25
Salt Lake City	5
San Antonio	13
San Diego	47
San Francisco	284
Schenectady	36
Seattle	42
South Bend-Mishawaka	10
So. Alberta	2
Syracuse	63
Tokyo	22
Toledo	8
Toronto	39
Tucson	10
Tulsa	21
Twin Cities	103
Vancouver	6
Washington	237
Wichita	6
Williamsport	1
Winnipeg	5
Total Paid Members	5325

Resume of PGEC Administrative Committee Meeting, February 27, 1957

The PGEC Administrative Committee met during the Western Joint Computer Conference in Los Angeles on February 27, 1957. In the absence of Chairman J. D. Noe, who was ill, Vice-Chairman W. Buchholz presided. Twelve voting members were present or represented by proxy. Several chapter and committee chairmen were welcomed as guests.

Secretary-Treasurer R. Y. Wing reported a financial balance of $24,920 as of December 31, 1956. Of this, $6,000 has been earmarked for the IRE Computer Fellowship for the next two years. Nearly $9,000 was spent on publications during the year. Not counting committed funds, the net balance increased by almost $1,000 during 1956.

The PGEC membership stood at 5494 at the end of 1956, including 498 student members.

Nominations Committee Chairman J. H. Felker presented a slate of new Administrative Committee members and officers for the coming year. There were no other nominations. Voting takes place during the March meeting.

The Committee approved a change in the PGEC by-laws to permit the PGEC Chairman to be elected during his third term on the Committee, so that he serves as Chairman during a fourth year and as Past-Chairman during a fifth year on the Committee. This follows a recent change in the PGEC Constitution permitting the Administrative Committee to consist of a maximum of 18 members instead of 15, as before.

Robert Roggenbuck from the Detroit Chapter was appointed to fill out the term of Norman Scott, who resigned.

The new IRE Affiliate plan was adopted for the PGEC. An initial list of professional societies whose members will be eligible to join the PGEC as nonvoting Affiliates and receive the PGEC Transactions (but not the IRE Proceedings) for a yearly fee of $6.50 includes:

- Association for Computing Machinery
- Society for Industrial and Applied Mathematics
- American Mathematical Society
- Operations Research Society of America
- National Association of Cost Accountants
- National Machine Accountants Association
- American Management Association
- Institute of Aeronautical Sciences
- American Physical Society
- American Society of Mechanical Engineers
- Society of Automotive Engineers.

The PGEC, for the time being, will not include advertising in the Transactions since the additional revenue is not needed.

Werner Buchholz

PGEC Administrative Committee Meeting

The following is a summary of the meeting of the PGEC Administrative Committee held in New York, N. Y., on March 18, 1957. A quorum of 13 members and proxies out of the 16 total members was present.

Meeting Notices

A letter from George Bailey, Executive Secretary, IRE, was read to the Administrative Committee, in which Mr. Bailey outlined the change in IRE requirements for publicizing Chapter meetings. Heretofore, in some Sections it has been considered essential to notify all members of the Section for every Chapter meeting, and the expense involved has prohibited the Section from paying for occasional meeting notices sent to

members of a particular Chapter. It is the PGEC Administrative Committee's present understanding that it is no longer an absolute requirement for the Section to notify all members for each meeting, therefore, it should be possible for the Section to handle the cost of an occasional special mailing to publicize a change in plan for a Chapter.

IRE Predoctoral Computer Fellowship

Dr. Willis H. Ware, Chairman of the Student Activities Committee, reported that the PGEC Fellowship is now officially established and the National Academy of Sciences is handling the fellowship for the PGEC. The award for the 1957–1958 fellowship is expected in April.

Funds for PGEC Chapters

The Committee approved a method of providing financial assistance to the PGEC Chapters, since it is now possible to send funds to a Section earmarked for a particular Chapter within the Section. The National PGEC will match IRE Headquarters' funds ($10 per meeting attended by more than 25 members, up to five meetings per year) for each PGEC Chapter meeting. Payment will be made upon submitting meeting reports, including date and number of people attending, to Stanley B. Disson, Chairman of the PGEC Sectional Activities Committee, Burroughs Corp., Great Valley Laboratories, Paoli, Pa.

Elections

New members and officers of the PGEC Administrative Committee were elected effective April 1, 1957. The results are tabulated inside the front cover of this issue.

Publications

As one of several moves to encourage the flow of worthwhile papers to the PGEC Transactions, the Committee reaffirmed the existing publication policy. Publication in a convention record or proceedings of a meeting shall not prejudice republication in the TRANSACTIONS, especially where the convention records or proceedings of the meeting are sent only to a small percentage of PGEC membership.

Next Meeting

The next meeting of the PGEC Administrative Committee will be held during WESCON in San Francisco during the period August 20–23, 1957.

JERRE D. NOE
Past Chairman, IRE-PGEC

Reviews of Current Literature

Copies of books or of articles to be reviewed should be sent to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*Harry D. Huskey*

GENERAL

57-31

Moderne Rechenmaschinen—Hans Bückner. (*Handbuch der Physik. Bd. II*, Springer-Verlag, Berlin-Göttingen-Heidelberg, pp. 471–498; 1955.) This review article is divided into two sections, covering analog and digital computers respectively. The emphasis is, rightly, on electronic internally-programmed digital calculators. The history of the subject is briefly outlined, from Babbage and Lady Lovelace till about 1954. A discussion of programming with examples of coding is based on the system used for the EDSAC in Cambridge, England. The logical structure of arithmetic operations in computers, use of binary numbers, representation of truth functions are among the theoretical topics. A section is devoted to the various kinds of memory employed.

W. Freiberger
Courtesy of *Mathematical Reviews*

57-32

Gedanken-Experiments on Sequential Machines—Edward F. Moore. (*Automata Studies, Annals of Math. Studies*, no. 34, pp. 129–153; 1956.) This paper studies distinguishability of sequential machines and distinguishability of internal states within a machine by experiments performed on the machines. It is shown that, for general machines, no finite experiment will suffice to identify one machine among the class of sequential machines (Theorem 2). By restricting the class of machines to those which are "strongly connected" and in "reduced form," it is then shown that there is some finite experiment with copies of a machine which will suffice to distinguish the machine from others in the class (Theorem 9). Several other theorems on distinguishability and on the length of experiments are proved.

C. Y. Lee
Courtesy of *Mathematical Reviews*

57-33

Some Uneconomical Robots—James T. Culbertson. (*Automata Studies, Annals of Math. Studies*, no. 34, pp. 99–116; 1956.) Using a number of each of three types of neurons, receptor, central, and effector, and with proper interconnection of these neurons, the paper shows how a memoryless robot can be constructed. Then, by chopping time into discrete levels and increasing the number of receptor and central neurons, it is shown how a robot with complete memory (a record, at any time t, of all past receptor firings) can be constructed. A way of introducing probabilistic behavior without inserting unreliable elements is also indicated.

C. Y. Lee
Courtesy of *Mathematical Reviews*

681.142 57-34

Design of Computer Circuits for Reliability—W. Renwick. (*Electronic Eng.*, vol. 28, pp. 380–384; September, 1956.) Factors influencing the choice of components, and precautions taken during the initial circuit design and mechanical construction of the EDSAC II machine are described.

Courtesy of Proc. IRE
and *Wireless Engineer*

57-35

The Application of Matrix Methods to Multi-Variable Control Systems—R. J. Kavanagh. (*J. Franklin Inst.*, vol. 262, pp. 349–367; November, 1956.) This paper presents the methods of matrix algebra which may be used for the description, analysis, and synthesis of the general ease of linear multivariable control systems. Some practical examples of the analysis and synthesis of systems are given and criteria for the realizability of multivariable control systems with desired characteristics are derived. The procedure adopted in this method is to describe the multivariable system by means of a matrix transfer function linking input to output. A computer matrix is then inserted between true inputs and the actual inputs to the multivariable system. The computer matrix forms linear combinations of the true inputs and the multivariable system outputs to form the desired actual inputs to the multivariable system. The synthesis problem reduces to the determination of the computer matrix elements. This paper is clearly written and provides information of considerable value to all who are engaged in the design of control systems, both analog and digital.

Gene M. Amdahl

57-36

The Mathematics of Information Theory—Brockway McMillan. (1955 IRE National Convention Record, pt. 4, pp. 48–51.) It seems superfluous to review an article which is itself nothing but a review of the broad aspects of a complex subject. Needless to remark, there is no mathematics in the article. There are no new approaches to any of the basic problems of information theory suggested; in fact, the limitations of present attempts at analysis are rather fatalistically accepted. The main point of the article is to observe that engineers and physicists have been working on the same problems as some mathematical statisticians, but with constraints which for some reason or other mathematical statisticians do not seem to permit themselves. Wald's work is lauded as a unifying force, but is observed to be responsible for more philosophizing than discovery. In short, this article will pass the censor's office, but will not be a big hit at the box office.

R. H. DeLano

57-37

The Vernier Time-Measuring Technique—R. G. Baron. (Proc. IRE, vol. 45, pp. 21–30, January, 1957.) This paper describes a technique for precision time measurement of the interval between two pulses. The system, which is accurate to 10 millimicroseconds, employs an electrical equivalent of the mechanical vernier scale to permit this accuracy while counting 2-mc pulses. This is accomplished by utilizing a coarse counter to count the 2-mc pulses between the start and stop pulses and a vernier counter to count the 2-mc pulses between the start or stop pulse and coincidence of a 2-mc pulse and a pulse from the vernier pulse generator. The vernier pulse generator is started by the start or stop pulse and produces pulses at a slightly greater rate than the 2-mc pulse generator until coincidence. The use of a single vernier frequency is made possible by proper control of the counter. In the interest of giving credit where credit is due, it should be noted that a paper, "Precision Automatic Time Measurement Equipment," was presented at the IRE National Convention, March 5, 1952, by D. W. Burbeck and W. E. Frady describing an almost identical system which was fabricated at Hughes.

A. D. Scarbrough

57-38

High-Speed Digital Conversion—M. L. Klein, F. K. Williams, and H. C. Morgan. (*Instruments and Automation*, vol. 29, pp. 1297–1302; July, 1956.) This is the third article of the series on analog-digital conversion by the authors. (See **56-158** and **56-159**, vol. EC-5, p. 261; December, 1956.) It is a survey of available equipment for high-speed data logging and digital conversion. The paper is divided into two sections, all-electronic data loggers and all-electronic high-speed converters. Four commercially available units are described in each category. Voltage conversion rates range from 20-100,000 per second with an accuracy of

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0.1 per cent. Block diagrams are given with a short outline of system operation. More detailed information in one or two cases would be helpful to the reader. However, the authors on the whole have presented a very excellent survey of existing equipment.

Raymond Davis

621.314.63+621.314.7 57-39

Maximum Power of Semiconductor Junction Elements—J. P. Vasseur. (*Ann. Radio-élect.*, vol. 11, pp. 3–28; January, 1956.) Universal curves are presented from which the maximum permissible power dissipation can be determined for Ge junctions cooled by 1) conduction or 2) convection. The influence of mounting, circuit arrangement, and signal waveform is discussed. The time taken to reach temperature equilibrium is investigated. Both diodes and transistors are considered.

Courtesy of PROC. IRE and *Wireless Engineer*

621.314.7 57-40

The Effect of Surface Treatments on Point-Contact Transistor Characteristics—J. H. Forster and L. E. Miller. (*Bell Sys. Tech. J.*, vol. 35, pp. 767–811; July, 1956.) The properties of formed point contacts on Ge are discussed; technique for observing the equipotentials surrounding such contacts is described. Differences between donor-free and donor-doped contacts are emphasized. Differences are also observed between unformed point contacts subjected to different surface treatments. These considerations are applied to a study of transistor point-contact forming in contemporary practice. High yields from the forming process can be expected with oxidized surfaces; the use of chemical washes to remove soluble Ge-oxide surface films greatly reduces the forming yields.

Courtesy of PROC. IRE and *Wireless Engineer*

621.314.63:546:28 57-41

Silicon Wide p-n Junction—J. Nishizawa. (*Sci. Rep. Res. Inst. Tohoku Univ., Ser. B*, vol. 6, pp. 183–215; 1955.) The effect of the depletion layer in Si *p-n* junctions is investigated by determining the *V/I* characteristics for various positions of the contact whisker, using a specially prepared junction having a very wide high-resistance layer.

Courtesy of PROC. IRE and *Wireless Engineer*

ANALOG COMPONENT RESEARCH

681.142 57-42

A Circuit for Analogue Formation of xy/Z—M. J. Somerville. (*Electronic Eng.*, vol. 28, pp. 388–389; September, 1956.) "A quarter squares multiplier, using a triangle carrier waveform in the squaring circuits is extended to give division simultaneously with multiplication. This is achieved by controlling the slope of the triangle carrier waveform so as to be proportional to the divisor Z."

Courtesy of PROC. IRE and *Wireless Engineer*

ANALOG EQUIPMENT

57-43

Aircraft Performance Studied on an Electronic Analog Computer—L. B. Wadel and C. C. Wan. (*Proc. Western Joint Computer Conf., Los Angeles, Calif.*, pp. 78–82; 1955.) The relations between aircraft performance (maximum speed, rate of climb, fuel consumption) aerodynamic data, and engine data are discussed. The analog computer components for the solution of these equations are outlined. The equations are mostly nonlinear algebraic, so function generators and multipliers are the most frequently used components. The complete computer is a cross between a special-purpose and a general-purpose analog machine. Some iterative techniques for computing range are mentioned. The computations have two uses: for the preliminary design of aircraft, and for presenting the performance data of the finished aircraft to the pilot in a handbook form. No consideration is made of desirable input-output equipment for the computer. This equipment is probably one of the most important parts for practical use of the machine. In addition no indication is given why an analog computer is superior to a general-purpose digital computer.

Max V. Mathews

57-44

On the Continuous Solution of Integral Equations by an Electronic Analog. I—Michael E. Fisher. (*Proc. Camb. Phil. Soc.*, vol. 53, pp. 162–174; January, 1957.) This paper describes the practical realization of a machine for solving a class of integral equations by analog techniques. It is based on an idea due to Wallman and uses an interesting device developed by Bergman for the storage and reproduction of analog waveforms. The machine can solve Fredholm integral equations of the second kind by a new form of iterative method which is claimed to be superior to that due to Neumann and the time taken for convergence is of the order of one second or less. Convergence and error analysis are discussed.

Stanley Gill

UTILIZATION OF ANALOG EQUIPMENT

57-45

The Representation of Constraints by Means of an Electronic Differential Analyzer—D. T. Greenwood. (IRE TRANS., vol. EC-5, pp. 111–113; September, 1956.) The use of high-gain amplifiers is shown to be helpful in the representation of constraints. This method enables one to represent constrained systems in a manner such that all coordinates are available for the application of arbitrary forces or displacements. The procedure is explained by means of an example.

Courtesy of PROC. IRE

DIGITAL COMPONENT RESEARCH

57-46

The Physics of Solid-State Light Amplifiers—D. A. Cusano. (IRE TRANS., vol. NS-3, pp. 102–106; November, 1956.) An essential component of present light amplifying screens is a layer of inorganic, luminescent material. The ability of this layer to derive energy from an electric field to which it is subjected and convert this energy into visible light (*i.e.*, electroluminescence) is fundamental to, but not alone sufficient for the realization of solid-state light amplification. What must be included is some means whereby the luminescent response to the field can be strongly controlled by incident radiation. In one case this has been obtained through the discovery of a phosphor film with the necessary properties, and in another by the utilization of a photoconducting material in contact with an electroluminescent layer. In the latter case the photoconductor is the radiation-sensitive element, which serves to modify the potential across the luminescent component.

The main characteristics of these light amplifying screens will be described, with particular emphasis on the interpretation of the phenomenon observed with the single phosphor film. The behavior, as it is relevant to their possible use in radiation detection, will be discussed.

Courtesy of PROC. IRE

57-47

Quarterly Report No. 12, Second Series—J. R. Bowman, C. H. T. Wilkins, *et al.* (*Quart. Rep. Computer Components Fellowship Mellon Inst.*, 45 pp.; July 1, 1956 to September 30, 1956.) In the first of these, the results of time and temperature studies on the preparation of printed enamel capacitors are discussed. Initial results obtained using a "flash evaporation" technique for the preparation of alloy resistor films by vacuum evaporation and deposition are reported in the second section. The third section contains descriptions of methods used for the preparation of stannic oxide resistor films. In Part II, changes in brightness wave characteristics that occur between 30 and 120 volts at 60 cps in electroluminescent cells having eight different metal backings are discussed. Over this voltage range, the disturbance ratio and the phase angle are found to be independent of the choice of electrode metal. Also, as the voltage is increased 1) the disturbance ratio decreased, 2) the modulation ratio decreased to zero then increased, 3) there is an over-all increase in the phase angle, but only in the nickel backed cell is this increase a smooth one.

C. H. T. Wilkins

57-48

A Study of the Neon Bulb as a Nonlinear Circuit Element—C. E. Hendrix. (IRE TRANS., vol. CP-3, pp. 44–54; September, 1956.) The ordinary NE-2 neon bulb possesses two-valued properties which make it valuable for use in logical gate circuits such as are used in digital computers. The cost of the NE-2 is of the order of $0.05 compared to an average unit cost of $1.00 for germanium diodes. In the logical gate application, circuit performance is relatively insensitive to parameter variations among bulbs. Both "or" and "and" gates, and combinations thereof can be built, and operation up to 30 kc easily obtained. Statistical studies of bulbs point out that the aging effects to be expected are a rise in voltage drop across the bulb and a reduction in the variability among bulbs. The change appears

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rather suddenly, after about 1000 milliampere-hours of operation. Equivalent circuits are presented, and simple circuit design techniques have been worked out.

Courtesy of Proc. IRE

57-49

Transmission Secondary Electron Multiplication for High-Speed Pulse Counting—E. J. Sternglass and M. M. Wachtel. (IRE Trans., vol. NS-3, pp. 29–32; November, 1956.) A new type of high-speed electron multiplier employing transmission secondary electron emission from thin insulating films is described. Electrons from a photosurface are multiplied in a series of plane-parallel dynodes consisting of a thin scattering layer of a heavy metal followed by a layer of a pure crystalline insulating material of high secondary emission yield. The characteristics of such dynodes are described and the dc and pulse performance of an experimental seven-stage device employing this principle is presented.

Courtesy of Proc. IRE

57-50

Supermendur, A New Rectangular-Loop Magnetic Material—H. L. B. Gould, D. H. Wenny. (*Electrical Eng.*, vol. 76, pp. 208–211; March, 1957.) This article discusses the characteristics of a vanadium (2 per cent)—iron (49 per cent)—cobalt (49 per cent) alloy named Supermendur. The electrical characteristics include: low coercive force, 0.26 oersted; low hysteresis loss; high maximum permeability, 66,000 at 20,000 Gausses; high remanence, 21,150; saturation 24,000 Gausses; flux swing 45,150. The article describes the melting, processing, heat treating, electrical tests, and structure of this material. The material has been rolled to thicknesses of 0.3 mil.

H. T. Larson

57-51

Modern Magnetic Ferrites and Their Engineering Applications—C. D. Owens. (IRE Trans., vol. CP-3, pp. 54–62; September, 1956.) Ferrites and their applications constitute a rapidly developing field. This paper reviews the present status of the development, properties, and applications of ferrites and their significance to modern engineering. Magnetic ferrites were developed from a "new look" at lodestone, the oldest magnetic material known to man. Proper control of composition and heat treatment yields ceramic type bodies with high permeabilities, which were formerly obtained only in metals. This material has brought the physicist new insight into the mechanisms of magnetism, and has given the design engineer a variety of new materials with unprecedented combinations of properties. The unique characteristics of ferrites are bringing about revolutionary design techniques in inductors and transformers for use at carrier, radio, and video frequencies, and have made possible an important new family of nonreciprocal circuit elements in microwave applications.

Courtesy of Proc. IRE

57-52

High-Speed Shift Registers Using One Core Per Bit—V. L. Newhouse and N. S. Prywes. (IRE Trans., vol. EC-5, pp. 114–120; September, 1956.) A three, and a two winding per core, high-speed, current driven, one core per bit shift register is presented together with an analysis of the basic circuit involved. An intermediate storage capacitor is used between successive logical elements. The charge and discharge of this capacitor are controlled in a positive manner by voltage blocking pulses. The undesired feedback of energy from one stage to earlier stages is thereby prevented, giving high efficiency of operation. The three winding per core register described is reversible and capable of operating in the megacycle range. The application of the basic shift register element to computer logic applications is described.

Courtesy of Proc. IRE

621.314.63 57-53

High-Frequency Silicon-Aluminum Alloy Junction Diodes—M. B. Prince. (IRE Trans., vol. ED-2, pp. 8–9; October, 1955.) A preliminary account of experiments on diodes made by alloying the point of a thin Al wire to a wafer of *n*-type Si; the diameter of the alloyed region is probably <0.0005 inch. Rectification at frequencies up to 500 mc has been obtained. The reverse saturation current is about 10^{-9} A.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.314.63:546.28 57-54

Reverse Current and Carrier Lifetime as a Fuction of Temperature in Silicon Junction Diodes—E. M. Pell and G. M. Roe. (*J. Appl. Phys.*, vol. 27, pp. 768–772; July, 1956.) Previous work on Ge diodes (Abstract 3424 of Proc. IRE, 1955) is extended to Si grown-junction diodes; measurements over the temperature range $-190°$ to $+200°$C are reported. The lifetime becomes constant over a low-temperature range; this is consistent with published recombination theory. The results indicate that charge generation from centers about 0.5 ev deep is responsible for most of the reverse current at temperatures up to well above room temperature.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.314.63 57-55

On the Transient Behaviour of Semiconductor Rectifiers—B. R. Gossick. (*J. Appl. Phys.*, vol. 27, pp. 905–911; August, 1956.) The investigation reported previously (Abstract 1236 of Proc. IRE, 1955) is extended to cover large-amplitude transients in surface-barrier and point-contact diodes.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.314.7:621.3.015.3 57-56

Theory of Transient Process in Semiconductor Triodes—E. I. Adirovich and V. G. Kolotilova. (*C. R. Acad. Sci. U.R.S.S.*, vol. 108, pp. 629–632; June, 1956. In Russian.) Expressions are derived for the transfer characteristics of a transistor operating in grounded-emitter and grounded-collector circuits. The corresponding expression for the grounded-base circuit was given previously. (Abstract 1892 of Proc. IRE, 1955.)

Courtesy of Proc. IRE
and *Wireless Engineer*

57-57

Logic Circuits for a Transistor Digital Computer—G. W. Booth and T. P. Bothwell. (IRE Trans., vol. EC-5, pp. 132–138; September, 1956.) The reliability and performance which can be achieved in high-speed switching circuits using presently available high-frequency junction transistors suggests the use of transistor circuits in preference to more conventional circuits for many applications. The area of airborne digital computers is one in which the physical characteristics of the transistor as well as of associated low dissipation components can be most favorably exploited. We have presented here a group of circuits which fulfill the requirements of speed, low dissipation, size, and weight for most such applications. The circuits shown will operate over the range $-30°$C to $+60°$C, and actually have been operated over the range $-50°$C to $-90°$C. Low dissipation of the circuits places minimum requirements on power supplies, and temperature control may be achieved with only a small amount of cooling. An estimate can be obtained from an example. For a large-scale computer, say 2000 transistors, 800 of which are in bistable circuits, total dissipation will be less than 140 watts.

Courtesy of Proc. IRE

57-58

Semi-Conductor Diode Amplifier Considerations—Henry W. Kaufman. (1955 IRE National Convention Record, pt. 4, pp. 146–149; 1955.) The author presents some experimental data on forward and reverse transients which was originally taken to aid in the design of conventional diode gating circuits. This data, which includes wafer thickness as a parameter, is then interpreted from the novel standpoint of the design of diode amplifiers. In one example, the author calculates that a circuit using a 1N191 input diode, a 1N92B amplifier diode, and a resistor will give an energy gain of about 18. This is for a one-microsecond input and a two-microsecond output pulse.

A. W. Holt

57-59

High-Speed Flip-Flops for the Millimicrosecond Region—Z. Bay and N. T. Grisamore. (IRE Trans., vol. EC-5, pp. 121–125; September, 1956.) The problem of designing high-speed flip-flops has been approached by dividing the circuit operation into steady-state and switching functions, the steady-state function being assigned to a slave flip-flop and the switching function to a driving circuit. Circuits, using conventional components and having a resolving time of 10 mμsec are described. Resolving times as low as 2 mμsec have been attained by using a special beam-deflection tube as the slave flip-flop. These circuits dissipate

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considerably less power in the intervals between switching than conventional circuits.

Courtesy of Proc. IRE

57-60

VHF Pulse Techniques and Logical Circuitry—D. E. Rosenheim and A. G. Anderson. (Proc. IRE, vol. 45, pp. 212–219; February, 1957.) This interesting paper presents techniques and components for handling 10 millimicrosecond pulses at 50 mc repetition rates. The active circuits make use of the Philips EFP-60 secondary emission pentode. The EFP-60 has an additional active electrode, the dynode which allows the tube to be used as a noninverting amplifier with both current and voltage gain and a grid to dynode transconductance of 20,000 μmhos The Western Electric 417A/5842 triode with $g_m = 25{,}000$ μmhos is used as a cathode follower for the fast pulses. Logical gating is performed with selected gold-bonded germanium diodes having high forward conductance and good transient response. Storage is accomplished by electromagnetic delay lines and EFP-60 reshaping circuits. A number of schematics of other computer circuits are given together with helpful hints on generating, observing, and transmitting these extremely fast pulses.

A. D. Scarbrough

537.226/.227:546.431.824-31 57-61

Polarization Reversal in the Barium Titanate Hysteresis Loop—R. Landauer, D. R. Young, and M. E. Drougard. (*J. Appl. Phys.*, vol. 27, pp. 752–758; July, 1956.) The af hysteresis loop of tetragonal $BaTiO_3$ is examined in relation to Merz's finding (Abstract 445 of Proc. IRE, 1955) that the rate at which the polarization reverses in an applied field of intensity E is proportional to $e^{-\alpha E}$, where α depends on temperature. The switching rate adjusts to variations in the applied field with a time lag whose order of magnitude does not exceed 10^{-8} sec. The results imply that domains cross the crystal with a speed of the order of that of sound. Increases in dielectric constant measured during switching remain unexplained.

Courtesy of Proc. IRE
and *Wireless Engineer*

537.226/.228.1 57-62

Effect of Hydrostatic Pressure on the Hysteresis Loop of Guanidine Aluminium Sulphate Hexahydrate—W. J. Merz. (*Phys. Rev.*, vol. 103, pp. 565–566; August, 1956.) Measurements at a frequency of 60 cps indicate that both the spontaneous polarization and the coercive field strength of this material increase with pressure up to about 500 atm.

Courtesy of Proc. IRE
and *Wireless Engineer*

537.226/.227 57-63

Ferroelectricity in Ammonium Sulphate—B. T. Matthias and J. P. Remeika. (*Phys. Rev.*, vol. 103, p. 262; July 1, 1956.) A brief note reporting that $(NH_4)_2SO_4$ becomes ferroelectric below its transition point at −49.5°C.

Courtesy of Proc. IRE
and *Wireless Engineer*

537.226/227:546.431.824-31:539.234 57-64

Time Changes in Thin Films of $BaTiO_3$—C. Feldman. (*J. Appl. Phys.*, vol. 27, pp. 870–873; August, 1956.) "The decrease of dielectric constant with time under an applied alternating field, less than the coercive field, has been studied in films of $BaTiO_3$ between 1 and 3 μ thick. The phenomenon may be interpreted as being associated with the process of switching the domains to a position more nearly parallel to the applied field."

Courtesy of Proc. IRE
and *Wireless Engineer*

537.226/.227:546.431.824-31 57-65

Switching Time in Ferroelectric $BaTiO_3$ and its Dependence on Crystal Thickness—W. J. Merz. (*J. Appl Phys.*, vol. 27, pp. 938–943; August, 1956.)"The switching time t_s and the switching current i_{max} have been measured as a function of applied field E and of the size of the sample. It has been observed that the "activation field" α for the nucleation of new domains is inversely proportional to the thickness of the sample. This behavior can be explained by assuming a surface layer. The thickness of this layer has been calculated to be of the order of 10^{-4} cm. The same way we can explain the thickness dependence of the 60-cps coercive field strength. Furthermore, it has been found that the switching time depends to a first approximation linearly on the thickness of the sample if the field E is kept constant. This can be explained by assuming a domain wall motion primarily in the forward direction or by assuming a nucleation mechanism. The maximum velocity of the domain growth was found to be of the order of the velocity of sound. The switching time does not depend on electrode area."

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142+621.397.5]:621.395.625 57-66

Recording and Reproduction of Frequencies above 100 kc/s on Magnetic Media. Application to Storage Elements and to the Recording of Television Images—R. Charlet. (*Rev. Gén. Élect.*, vol. 65, pp. 359–365; June, 1956.) A combined summary of papers presented at a conference on the recording of sound and information held in Paris in April, 1955; current techniques are described and necessary improvements are indicated.

Courtesy of Proc. IRE
and *Wireless Engineer*

57-67

500,000,000—Bit Random—Access Memory—George E. Comstock. (*Instruments and Automation*, vol. 29, pp. 2208–2211, November, 1956.) This paper describes a large random access memory. The storage medium is standard $\frac{5}{8}$-inch instrument—quality Mylar-base magnetic recording tape. Strips of tape approximately two feet long are strung vertically on stainless steel frames. About 40,000 feet of tape are accessible on a random basis within less than a second, with average access time less than $\frac{1}{2}$ second.

Raymond Davis

DIGITAL SYSTEMS RESEARCH

57-68

A Topological Method for the Determination of the Minimal Forms of a Boolean Function—R. H. Urbano and R. K. Mueller. (IRE Trans., vol. EC-5, pp. 126–132; September, 1956.) The topology of the n-dimensional cube is used to reduce the problem of determining the minimal forms of a Boolean function of n variables to that of finding the minimal coverings of the essential vertices of the basic cell system associated with the given function. The proof of this statement is contained in the central Theorem 4. A numerical easily programmed procedure is given with which it is possible to treat problems with a greater number of variables than has heretofore been practical. The procedure bypasses the determination of the basic cells (the prime implicants of W. V. Quine) and locates the essential vertices, from which in turn the irredundant and minimal forms are obtained.

Courtesy of Proc. IRE

57-69

Circuit Minimization: Minimal and Irredundant Boolean Sums by Alternative Set Method—E. W. Samson and R. Mueller. (*Communications Laboratory, Electronics Research Directorate*, AF Cambridge Res. Center, Cambridge, Mass., Tech. Rep. 55–109, v+11 pp.; 1955.)

Circuit Minimization: Sum to One Process for Irredundant Sums—E. W. Samson and R. K. Mueller. (*Communications Laboratory, Electronics Research Directorate*, AF Cambridge Res. Center, Cambridge, Mass., Tech. Rep. 55–118, vii+16 pp.; 1955.) The problem of simplifying switching circuitry is closely allied with the problem of simplifying truth functions, and has given rise to investigations of Boolean functions and Boolean matrices. The authors, beginning with the analysis by Quine (*Amer. Math Monthly*, vol. 59, pp., 521–531; 1952, MR 14, 440) have developed an algorithm which tests whether a Boolean function is equal to one. This "sum-to-one" process is based upon the following theorem: if a_j, b_k, c_l and R are Boolean functions not involving the Boolean variable s explicitly, then

$$s \sum_j a_j + \bar{s} \sum_k b_k + \sum_l c_l \geqq R$$

if and only if $\sum_{j,k} a_j b_k + \sum_l c_l \geqq R$.

This sum-to-one algorithm is then applied to find all minimal and irredundant Boolean sums equivalent to a given Boolean Function. It seems to the reviewer that the method of application of the basic algorithm to the main problem could be considerably clarified by, for example, attempting to program it for some automatic computer.

S. Gorn

Courtesy of *Mathematical Reviews*

57-70

A Note on Microprogramming— Herbert T. Glantz. (*J. Assoc. Comp. Mach.*, vol. 3, pp. 77–84; April, 1956.) Since the term "microprogramming" was introduced early in this decade, the word has become widely used, but with many different meanings. Unfortunately, in most cases, the use of the

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term has not occurred in the technical literature—a situation which has retarded the development of a common definition throughout the field. Hence, it is considerable service in itself that the author has chosen to publish his interpretation of this technique. In discussing this concept. the author suggests that a possible criticism of current commercial machines is that there is a certain lack of versatility which arises from the customary fixed set of commands which provide for the use of only a fraction of the total possible different sequences of combinations of the internal operations of the machine. On the other hand, the essential characteristic of a microprogrammed machine is that it permits the programmer, in one manner or another, to manufacture his own command which could produce whatever sequence of combinations of internal operations he might desire. These arbitrary sequences are produced in the example which he discusses by placing a particular serial-parallel pattern of binary characters in a magnetic core memory. A control command which initiates the sequential read-out of this pattern into appropriate control circuits initiates the desired operation. Although it lacks any rigorous analysis of the possible advantages or disadvantages of such a system as compared to more conventional ones, and the definitions may be considered to be incomplete, this article represents a considerable contribution to the common understanding of this technique.

Gordon Morrison

57-71

Reliable Circuits Using Less Reliable Relays, Part I—E. F. Moore and C. E. Shannon. (*J. Franklin Inst.*, vol. 262, pp. 191–208; September, 1956.) The full paper describes an investigation made of relays whose reliability can be described in simple terms by means of probabilities. It is shown that by using a sufficiently large number of these relays in the proper manner, circuits can be built which are arbitrarily reliable, regardless of how unreliable the original relays are. In Part I, it is shown that if relay contacts may be characterized by the probability a of some closing when the coil is energized, and with probability c of others closing when the relay is not energized, then a highly reliable computer may be constructed from these relays if and only if $a \neq c$. A set of theorems are proven which make possible the design of a network in which a series of contacts may be replaced by the network and have the probability $h(a)$ of the contacts being open when energized be less than $\frac{1}{2}$ and the probability $h(c)$ of the contacts being open when not energized be greater than $\frac{1}{2}$.

Gene M. Amdahl

57-72

Reliable Circuits Using Less Reliable Relays, Part II—E. F. Moore and C. E. Shannon (*J. Franklin Inst.*, vol. 262, pp. 281–297; October, 1956.) Part II develops a three-step procedure for designing a relay network of arbitrary reliability. The first step consists of finding a network which for a given a and c makes $h(a) < \frac{1}{2}$ and $h(c) > \frac{1}{2}$. The second step consists of finding networks for which $h[h(a) < \frac{1}{2}] \leqq \frac{1}{4}$ and $h[h(c) > \frac{1}{2}] \geqq \frac{3}{4}$. The third step consists of finding networks which take these probabilities of $\frac{1}{4}$ and $\frac{3}{4}$ or better and move them arbitrarily close to 0 or 1 respectively. The results of these procedures are compared with von Neumann's results using the Sheffer stroke organs. For an individual contact (or Sheffer stroke organ) error probability of 0.005, to achieve a circuit error probability of about 10^{-20}, a redundancy of about 100 to 1 is required with contacts but about 60,000 to 1 is required with Sheffer stroke organs.

Gene M. Amdahl

57-73

Digital Process Control—M. L. Klein, F. K. Williams, and H. C. Morgan. (*Instruments and Automation*, vol. 29, pp. 1979–1984; October, 1956.) This paper discusses briefly the general problem of closed-loop automatic control systems. The problem of constructing a digital control system is presented. As an example a digital control system is designed to control a simple chemical process in which it is required to control the temperature at one point and the pressure at two points. The solution is a fixed program machine. The material is well presented; however, some mention might have been given of stored program machnies for ditigal control applications.

Raymond Davis

DIGITAL EQUIPMENT

57-74

Rechenautomaten im Dienste der Technik. Erfahrungen mit dem Zuse-Rechenautomaten Z4—Eduard Stiefel. (*Arbeitsgemeinschaft für Forschung des Landes Nordrhein-Westfalen.* No. 45, pp. 29–45, discussion pp. 47–65; 1955.) This is mainly a report on the work done and the experience gathered with the low-speed, small-memory relay computer Z4 when tabulating functions, solving polynomial equations, linear and nonlinear differential equations, partial differential equations, eigenvalue problems, etc. The author emphasizes that a general-purpose computer, used for problems of various length and complexity, will be useful only if its speed is matched by adequate in- and output facilities and if programming is as easy as possible. This has led to the following requirements for the new machine (ERMETH) replacing Z4: 1) ERMETH is a decimal machine throughout with floating point arithmetics. 2) The "coding box" on which codes will be punched will show the conventional mathematical symbols (+, −, ×, ÷ etc.). 3) A few simple orders together with a "Small Manual" will suffice for the simple computations of "novices," but additional facilities will be available for "experts." After the lecture, H. Behnke, L. Brandt, G. Hoheisel, H. Kaiser, J. von Neumann, E. Sperner, E. Peschl, H. Peterson, R. Sauer, E. Stiefel, A. Walther and W. Weizel discussed various aspects ranging from storage devices and analogy machines to economics and training of mathematical personnel.

H. H. Goldstine

Courtesy of *Mathematical Reviews*

57-75

The G-15 Digital Computer—S. Herbert Lewis. (*Instruments and Automation*, vol. 29, pp. 1773–1779; September, 1956.) This paper was presented at the Second Computer Clinic, Second International Automation Exposition, Chicago, Illinois, 1955. It is an introduction to the principles, operation, and application of a general-purpose digital computer. The author does a good job of explaining to the novice what a general purpose computer is supposed to do. Elementary binary arithmetic is presented in a clear manner. After this introduction the major elements of a general purpose computer are described in terms of the G-15 machine. The command word structure is given; however, the list of the commands available in the G-15 are omitted. Programming techniques are well covered and a typical flow chart is presented. Subroutines, scaling, and optimizing access time are briefly explained. A highway construction problem is taken as an example of a problem which illustrates the capabilities of the G-15 computer. The author has succeeded in writing a clear and understandable paper for the reader who has no previous knowledge of the digital computing field.

Raymond Davis

57-76

The UNIVAC and UNIVAC Scientific—W. Allen and G. E. Smith. (*The Computer Handbook*, ed. by Milton H. Aronson, The Instruments Publishing Co., Pittsburgh, Pa., pp. 46–55; 1955.) Brief descriptions are provided of the functions and interrelationships of the major components of the UNIVAC and UNIVAC Scientific (formerly ERA 1103) computing systems, including input-output and auxiliary equipment. The instruction repertories are described in general terms but are not listed in detail. Some fields of application of the two computer systems are indicated, emphasizing the commercial uses of the UNIVAC and the scientific uses of the UNIVAC Scientific. A few simple examples are presented of the use of some of the special coding features of the UNIVAC Scientific.

E. Bromberg

57-77

Digital Time and Sequence Control—M. L. Klein, F. K. Williams and H. C. Morgan. (*Instruments and Automation*, vol. 29, pp. 2403–2407; December 1956.) The paper deals with the application of digital techniques to time and sequence control problems. The circuits of a variable-interval automation control are clearly discussed.

Raymond Davis

57-78

Digital Telemetering and Print-Out of Pipeline Information—M. T. Nigh. (*Electrical Eng.*, vol. 76, pp. 216–219; March, 1957.) In the past, common methods of telemetering pipeline information have been the time-impulse method and variation of the frequency of a signal proportional to the measured variable. These are analog methods. Noise or signal interruption cause disturbing readings on dispatcher recorders. This article describes a system which con-

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verts readings to digital form at the source and transmits binary-coded decimal information to a central station. The system includes provisions for rejecting nonsense information. A system now in operation signals twelve different conditions at a remote pumping station, including seven malfunction conditions, with a few of these malfunction indications really representing a set of several malfunctions. The station also signals when deviations of certain variables exceed preset amounts, and when the rate of change of certain variables exceeds present amounts, either case causing automatic print-out in an electric typewriter at the central station. The transmitters and encoders are described in general terms—no circuits. Telephone transmission lines are used. Bits are transmitted as long or short pulses. These channels can be used for transmitting control signals back to the remote station.

H. T. Larson

UTILIZATION OF DIGITAL EQUIPMENT

57-79

Programming the Computer—S. M. Rock and W. W. Klammer. (*Control Engineering*, vol. 4, pp. 119–123; March, 1957.) This paper describes the various steps involved in preparing a program for scientific and, particularly, business problems. It mentions the formulation and numerical analysis of scientific problems very briefly, but concentrates mainly on the formulation and programming of business data processing problems. The article describes how the general analysis of a business problem might be performed using check reconciliation, as an example, specifying how the memory space must be assigned for the program and each type of input and how the detailed flow chart is prepared from which the individual program steps are written. The authors present an example of a program for the bank (check) reconciliation problem. They then describe debugging operations and the various alternatives available here; such as a program comparing computer results with manually obtained results in a checking routine, monitoring programs, and "post mortems." They describe how the "B register" or "index register" is used, and briefly discuss subroutines and automatic programming. The article is an excellent, but brief, description of the operations involved in preparing programs for business applications.

Neal J. Dean

57-80

Office Automation—W. F. McCelland, D. R. Jarema, and R. M. James. (*Instruments and Automation*, vol. 29, pp. 2426–2430; December, 1956.) The authors have divided this paper into three sections, a general discussion of linear programming and simulation, and two specific applications of the IBM 650 data processing system. The linear programming discussion is centered around the savings that might be achieved by applying this mathematical tool to business problems. No attempt is made to explain the techniques involved. Both of the installations, one at the A. C. Nielson Company, and the other at Montgomery Ward, have replaced punched card equipment. No major procedural changes were made. The A. C. Neilson Company is processing market research data and Montgomery Ward is using the 650 to prepare operating budget and profit and loss statements.

Raymond Davis

BOOK REVIEWS

57-81

Analog Computer Techniques—C. L. Johnson. (McGraw-Hill Book Co., New York, N. Y., 246 pp.+6 index+11 appendix+xi; 1956.) The material covered in this book should be a valuable aid to users and operators of dc electronic analog computing equipment. As the author points out, the analog computer and the digital computer become much more effective tools for the engineer, the scientist, and the mathematician when he understands the principles of operation of such equipment and has a working knowledge of the techniques involved in its utilization. Brief, but in general, adequate descriptions are given of the principles of operation and design of the computing components which comprise present day analog computers. In view of the rapid changes occurring in the state of the art, references made by the author to the characteristics of components in commercially available computers must be accepted by the reader largely as examples for the point being made by the author, rather than as information on the capability of the latest available equipment. Good discussions are presented on how to program problems including the considerations of time scale, amplitude scale, linear and nonlinear function representation, problem stability, and computer stability. One chapter presents the techniques involved in using an electronic differential analyzer for special applications such as solving algebraic equations, partial differential equations, and eigenvalue problems. Control and checking features included in present-day computers are summarized. The use of numerical analysis techniques and digital computers as auxiliary tools for analog computer checking is also covered. Two chapters at the end of the book are devoted to related-type computing equipment; there is a discussion of the principles of operation of the repetitive type analog computer and of the digital differential analyzer. It should be noted that two or three areas of computer operation are not included in the book. Although the drift and bandwidth problems are touched on in the discussion of time scale, certain mathematical and graphical information should be available to the operator so that he may more readily adapt his problem to the computer and also chose a computer for his problem. The latter consideration requires a discussion of using analog computers for real time simulation. More information should have been provided regarding coordinate systems and vector transformations. It would have been helpful also for the book to include a discussion of ac electromechanical differential analyzers and passive network analyzers. The author is to be congratulated for his accomplishment of assembling in one place the techniques which are being used by most of the large analog computer operating groups, in some cases, as written instructions, but most often as operator trade secrets. Although the book is written as a text for an introductory course on using analog computers, it should prove valuable to computer operators and users out of the class room.

C. M. Edwards
Courtesy of PROC. IRE

57-82

Automatic Digital Computers—M. V. Wilkes. (John Wiley and Sons, New York, N. Y., 305 pp.+x; 1956.) This book is a good survey of the digital computing field. Being a survey, it will probably not satisfy each specialist in his own line, but it will give him a good understanding of the problems arising in other lines. As the author states, the book will not enable a competent computer-programmer to design automatic digital computers, nor will it enable a computer designer to become a competent computer programmer. The book contains excellent sections on the history of automatic computers, the design of many of the present computers, the philosophy of coding, and the philosophy of computer design. The author goes quite deeply into the electronic circuitry of computers and into coding techniques in order to delineate the still unresolved controversies, such as serial against parallel design and automatic machine compiling of programs against direct coding in machine language. The typography is clear and the illustrations both profuse and of good quality. One of the most valuable contributions is the comprehensive annotated bibliography. This book should certainly be in the library of every large-scale computing facility and will be of real interest to all who are associated in any way with the digital computing field.

John E. Maxfield
Courtesy of *American Mathematical Monthly*

57-83

Handbook of Semiconductor Electronics—Edited by L. P. Hunter. (McGraw-Hill Book Co., New York, N. Y., 132 pp.+13 index+68 bibliography+xxviii; 1956.) This book, which includes sections by fourteen contributors, is the result of an effort to collect together the major principles in the semiconductor electronics field. An idea of its scope can be obtained from the table of contents. There are twenty sections distributed among four main divisions: physics of transistors, diodes, and photocells; technology of transistors, diodes, and photocells; circuit design and application for transistors, diodes, and photocells; and reference material. Section headings are: 1) Transistor Characteristics; 2) Electronic Conduction in Solids; 3) Rectification in Solids; 4) Transistor Action; 5) Photoconductivity and Photovoltaic Cells; 6) Preparation of Semiconductor Materials; 7) Methods of Preparing *PN* Junctions; 8) Metal-Semiconductor Contacts; 9) En-

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capsulation; 10) Device Design Considerations; 11) Low-Frequency Amplifiers; 12) High-Frequency and Video Amplifiers; 13) Directly Coupled Amplifiers; 14) Transistor Oscillators; 15) Transistor Switching Circuits; 16) Circuits Using Special Semiconductor Devices; 17) Graphical Analysis of Nonlinear Circuits; 18) Matrix Methods of Circuit Analysis; 19) Measurement of Semiconductor-Device Parameters; 20) Measurement of Material Parameters. An extensive bibliography of the transistor, semiconductor, and rectifier fields covering the period 1940–1955 inclusive closes the book; this bibliography is the most comprehensive listing in print for these fields. As its title indicates, the book is organized as a handbook, simplifying the location of desired information but carrying with it the disadvantage of small type, the same size as that of this review. There are very few typographical errors. The excellent selection and balance of topics, and the lack of appreciable duplication of material in sections written by different contributors are a tribute to the editor's skill and patience. All the contributions are authoritative and reflect the wide experience of their authors. Especially noteworthy, however, are the initial sections on the physics of semiconducting devices, the section on low-frequency amplification, and that on transistor switching circuits. Many of the sections depart from being strictly a collection and discussion of past work and in addition include valuable material unavailable elsewhere. It will be a rare worker in the semiconductor field who will not find much to learn from the book. Nevertheless, its topics are so well developed from basic principles that the newcomer to semiconductors may use it to familiarize himself with almost any subject in the area. The book fulfills its aims very well, may be highly recommended, and is likely to remain for some time the standard reference in this rapidly growing field.

J. R. Macdonald
Courtesy of Proc. IRE

57-84

Handbook of Industrial Electronic Control Circuits—J. Markus and V. Zeluff. (McGraw-Hill Book Co., New York, N. Y., 352 pp.+8 index+xiv; 1956.) Engineers who have made use of the 1948 edition of Markus and Zeluff's *Handbook of Industrial Electronic Circuits* will be delighted to know that a sequel, *Handbook of Industrial Electronic Control Circuits*, is now available. This handbook, the fifth by these electronics editors, fully lives up to and probably will somewhat enhance the reputation established by its predecessors. As electronics engineers well know, much that is worthwhile in the way of industrial electronics circuits has been published since 1948 but the problem of finding just what one wants when it is needed is a burdensome one and this reviewer for one finds it utterly impossible to remember all the circuits that are of frequent use, much less those that involve only occasional use. This book then brings together in conveniently indexed form most (perhaps all) of the circuits published in *Electronics* during the years 1948 to 1956 which are of primary interest to the industrial electronics engineer. As in its predecessor volume, each circuit is accompanied by a concise description giving the general nature of the circuit, an explanation of how it works, data on critical components, and suggested applications. New circuits are included under most of the main subject titles used in the 1948 book and four new subjects—radiation circuits, remote control circuits, sorting circuits and transistor circuits—are introduced. Transistor circuits in particular, were just not in existence prior to 1948 but forty circuits are included in this issue and the list seems to encompass just about everything suitable for use in the industrial field, plus some that are probably of use solely in communications work. Even so, the transistor application field is so new that further expansion of this section would be a very fine thing. It is interesting to note that no limiter circuits were published between 1948 and 1956, but in such a well-developed field as motor control twenty-three new circuits are shown. This handbook, like its predecessor, is intended primarily for experienced engineers working in the industrial electronics field. Instructors of industrial electronics courses will find it valuable as a reference book and recent graduates will find it of great help in bridging the gap between college theory and practical circuit design. This reviewer was disappointed not to find at least one good memory circuit for use in automatic test equipment, also a good thermocouple temperature controller circuit, but apparently these are yet to appear anywhere. In a few cases, notably the neon lamp flip-flop circuit on page 77, the description is oversimplified to the point of not warning about change of characteristics of the neon tube with time; hence, it may lead to disappointment if followed too literally. All in all, the book is extremely well done and fills a very substantial and rapidly growing need in its field.

C. A. Priest
Courtesy of Proc. IRE